Silicom

Silicom Denmark A/S FPGA SOLUTIONS

Connectivity Solutions

FB4XXVG@Z21D FPGA Card

Quad Port SFP28 25 Gigabit FPGA Card

Product Description

The FB4XXVG@Z21D is a high-performance OEM hardware platform intended for hardware acceleration for mobile 4G and 5G Baseband Units or Distributed Units with four SFP28 modules. Example: supports up to 16 100MHz carriers Radio Units via 4x 25G eCPRI/CPRI with SFP28 modules, as well as interfacing to a Grand master via SFP28 at 1/10/25G.

The card is based on a Xilinx® Zynq UltraScale+ RFSoC, which embeds a Processor System (PS) with four 64-bit Application Processing Units (ARM Cortex-A53) and two Real-Time Processing Units (ARM Cortex-R5) along with a powerful Programmable Logic (PL) part (UltraScale+ FPGA), as well as an integrated SD-FEC block.

The design is set to work in ORAN LLS-C1 and C2 with the intention to be utilized with a 4G/5G IP stack interfacing at 3GPP functional split options 8 for CPRI or 7.2x for eCPRI.

Key Features

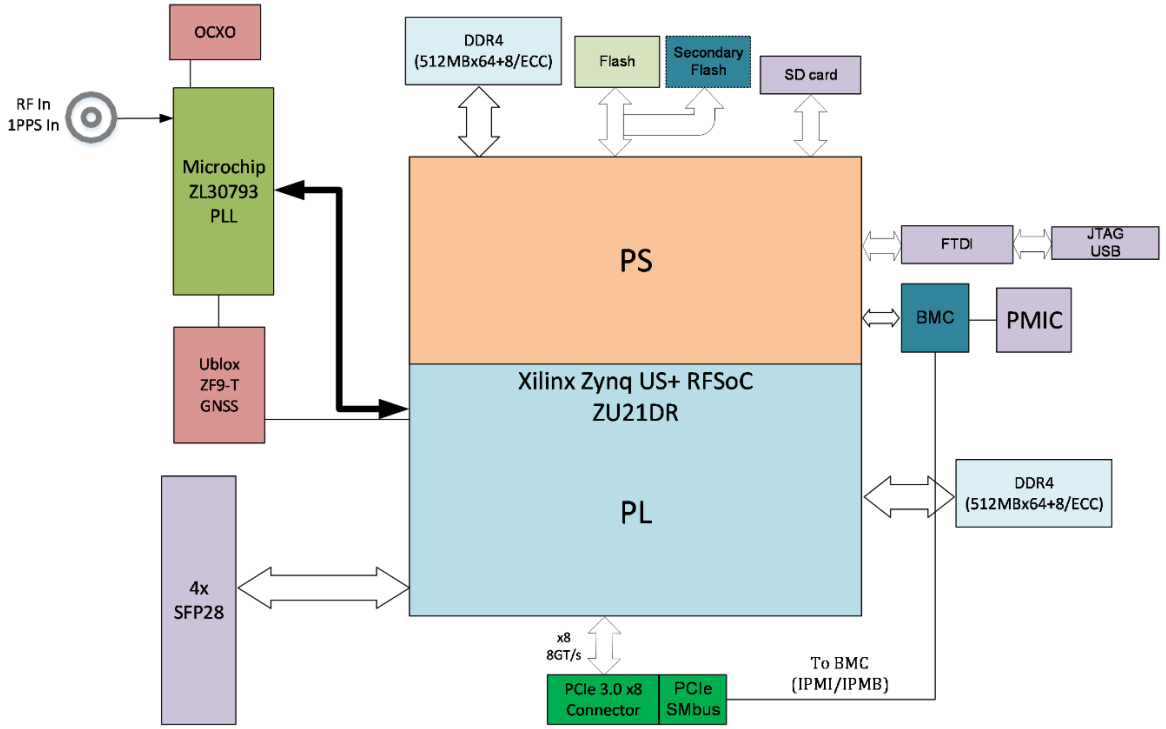
- FPGA ZU21DR Speedgrade -1
- 4x SFP28 (1/10/25GB) (usable for PTP/sync)
- 1x 4GB DDR4 for Programmable Logic (FPGA)
- 1x 4GB DDR4 for Processing System (CPU)
- Dedicated HW for IEEE 1588 PTP support
- IEEE 1588
- Support for SyncE
- Support for extended holdover time with high stability clock OCXO
- GNSS receiver with bias for external antenna with 1x SMA connector or optional 1PPS input
- Optional secondary extension bracket with 2xSMA (1PPS In/out), 2xSMA (10MHz in+out)
- PCIe 3.0 x8
- Passive cooling (Active solution on request)
- Full height, Half length

Technical Specifications

Network Interface	
IEEE standard	▪ IEEE 1588-2019
Interfaces	▪ Physical interface: 4x SFP28 ▪ Supported SFP28 and SFP+ ▪ SMA connector to active GNSS Antenna
Host Interface	
PCI bus	▪ 8 lanes PCIe Gen1/Gen2/Gen3

General Technical Specifications	
Configuration	▪ Upload of FPGA and SW code to flash via USB-JTAG ▪ Upload of FPGA and SW code to flash via micro-SD card ▪ Upload of FPGA and SW code to flash via PCIe host interface ▪ Support for encrypted FPGA bit file (optional)
On-board Memory	▪ 1x 4GB DDR4 (with ECC) for Programmable Logic (FPGA/PL) ▪ 1x 4GB DDR4 (with ECC) for Processing System (CPU/PS)
On-board Clock	▪ PCIe clock: 100 MHz (from host) ▪ Microsemi ZL30793 PLL ▪ PLL generated: Programmed ▪ OCXO for PTP
RFSoC Versions Available	▪ XCZU21DR—1FFVD1156E ▪ XCZU21DR—2FFVD1156E
Environment	▪ Physical dimensions: Half length, standard height PCIe ▪ Power consumption: Max 65W ▪ Operating temperature: 0 – 55°C, 30 – 130°F ▪ Operating humidity: 20 – 80%, non-condensing ▪ Hardware compliance: RoHS, CE ▪ Passive cooling (no on-board fan required)
Additional Board Support	▪ On-board temperature sensors ▪ Board status LEDs ▪ FPGA controlled Link and Activity LED for each port ▪ PPS clock synchronization connector (option) ▪ EEPROM storage ▪ Configurable PLL clock synthesizer (support for SyncE) ▪ 10MHz high stability oscillator

High Level Hardware Block Diagram



Description

Silicom Cassino Design employ a Xilinx RFSoC ZU21DR FPGA with no DAC/ADC hence optimized for High Phy (and Low Phy) implementation with 8 SD-FEC Cores for FEC Offload (LDPC, Turbo), by that freeing all the 930K System Logic Cells and 4272 DSP Slices for a layer 1 offload. The board is design with a 4GB (with the ability to expand to 8GB) DDR4 memory x72 (x64 with ECC) banks for PS and PL providing the user with enough memory for building deep FIFO. 4x SFP28 ports provides 25GbE connectivity to RRH with the support of PTP and SyncE while the Quad Core A53 enables PTP/1588 Termination on Smart NIC to ease system design.

Feature	Description	Notes
Form Factor	PCIe Form Factor, Full Height;Half Length	
Cooling Solution	Passive	
Operating Temperature	0ºC to +55ºC	
NEBS	Level 3	
Ports	4x SFP28	
Data Rate	10GbE and 25GbE Support Fiber (25GBASE-SR, 25GBASE-LR,25GBASE-CR), SFP(+/28) Direct Attach	
Host Interface	PCIe 3.0 x8	
FPGA	Xilinx ZU21DR -2/-1 SG	
Memory	PS 4GB (with option for 8GB) PL 4GB (with option for 8GB)	
PLL	Microchip ZL30793	
SMA	RF Input 1PPS Input	1x SMA Connector, Dual function Option - 1PPS In/Out and 10Mhz In/out on a Separate metal bracket
GNSS	Ublox ZF9T	Optional
OCXO	SiTimes SIT5721AC-KW333-T-10.00000T MicroSemi OX-4011-EAE-0580-20M000 MicroSemi OX-2281-EAE-5000-20M000	Only one of them is assembled
BMC	Silicom Standard Gecko - Telemetry, Flash Control, Power Sequencing	
Regulation	CE, FCC Class B, ROHS, REACH, CMRT, UL	

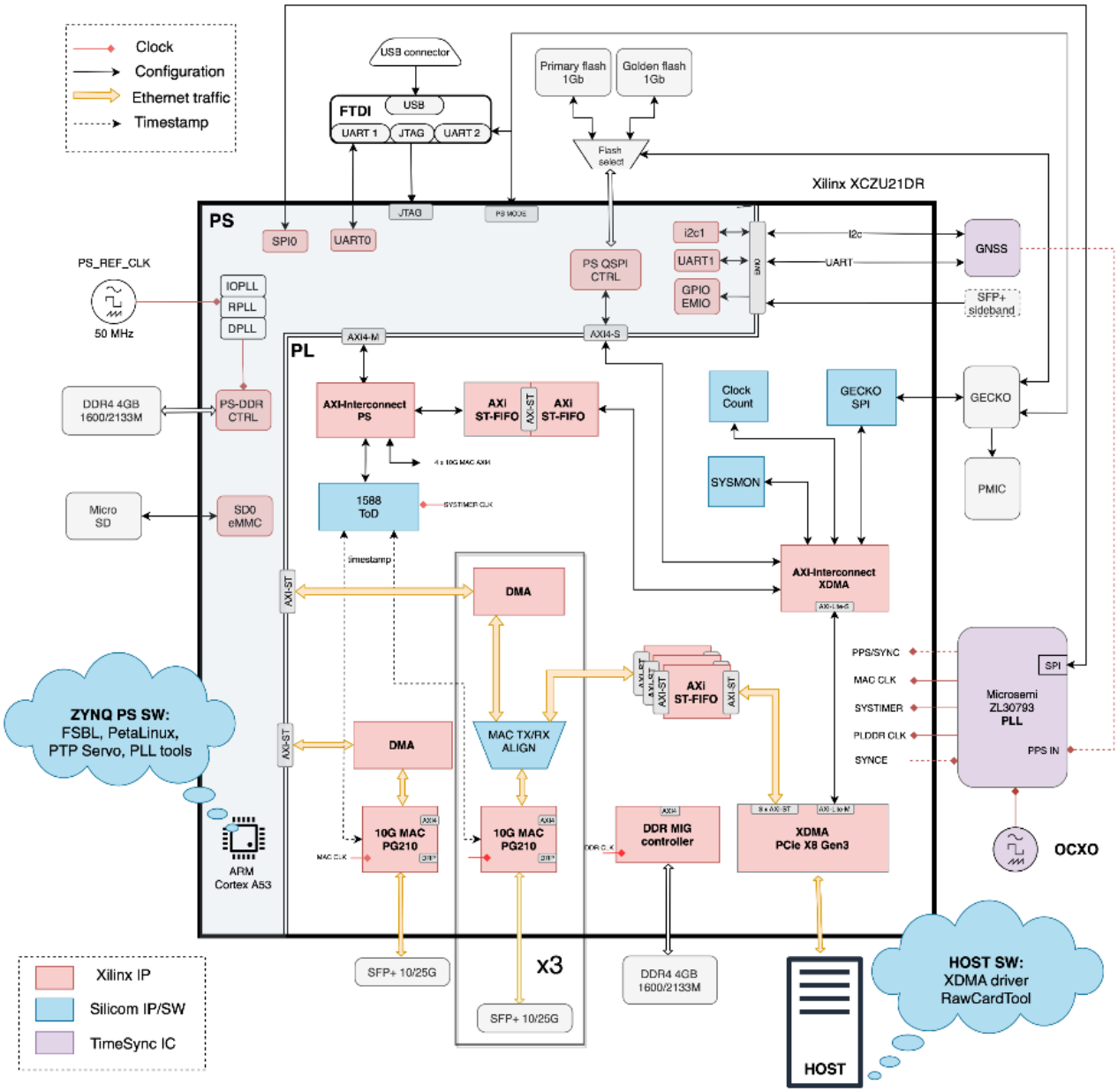
Silicom Demo Design

Silicom Demo Design is a basic image Silicom provide with the hardware that serves as a start point for development.

- Full reference design with data wire to host
- Flash Programming from host – over PCIe
- XDMA to PCIe Gen3
- 1 x Configuration AXI-Lite Master Interface: Access to the QSPI Flash device from HOST, accessing BMC and telemetry data from HOST, HOST to PS and PS to HOST file transfer
- 3 x AXI-ST interface: Streaming data packets between the front ports (SFP+ 10G) and HOST

Features

- 4x 25GbE/10GbE
- XDMA to PCIe
- PTP Time Stamp
- Memory Controller in PS/PL
- SD Card to PS for Debug
- PS Data path via 10G Ethernet ports
- AXI Interface
- I2C access via host SMBus



Cassino Deliverables

Software Repository which includes

- Data Plane (PCIe)
  - XDMA Driver
- Card Management tool
  - BMC – Board Management Controller
  - Flash programming
  - Monitoring
  - Statistics and debug
- Xilinx Petalinux running on ARM Cores (PS)
- Time Synchronization PTP/1588 Stack and Servo SW (PS)

Hardware

- 1x Cassino card
- 1x USB cable (JTAG) – optional
- 1x SMA Cable – optional
- 1x SMA Bracket with 1PPS Input/Output and 10Mhz Input/Output – optional
- 4x Fiber (25GBASE-SR, 25GBASE-LR,25GBASE-CR), SFP(+/28) Direct Attach - optional

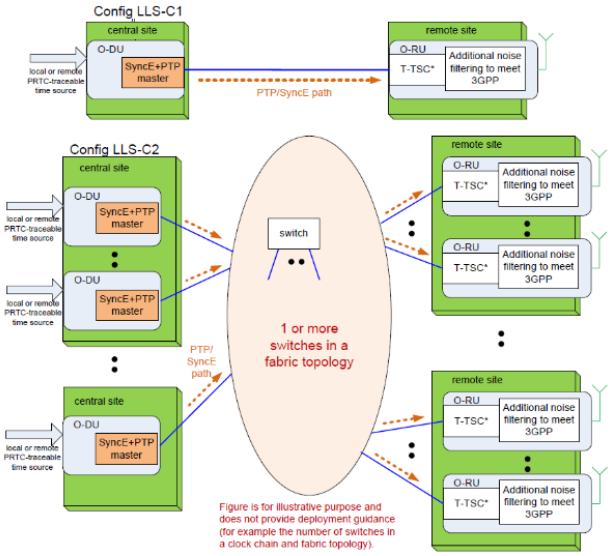
Documentation

- Hardware Specification
- Installation User Guide
- Demo Design User Guide
- SDK Reference Manual
- Petalinux User Guide
- Raw card tool Guide

Cassino Time Synchronization Sub System

Standards

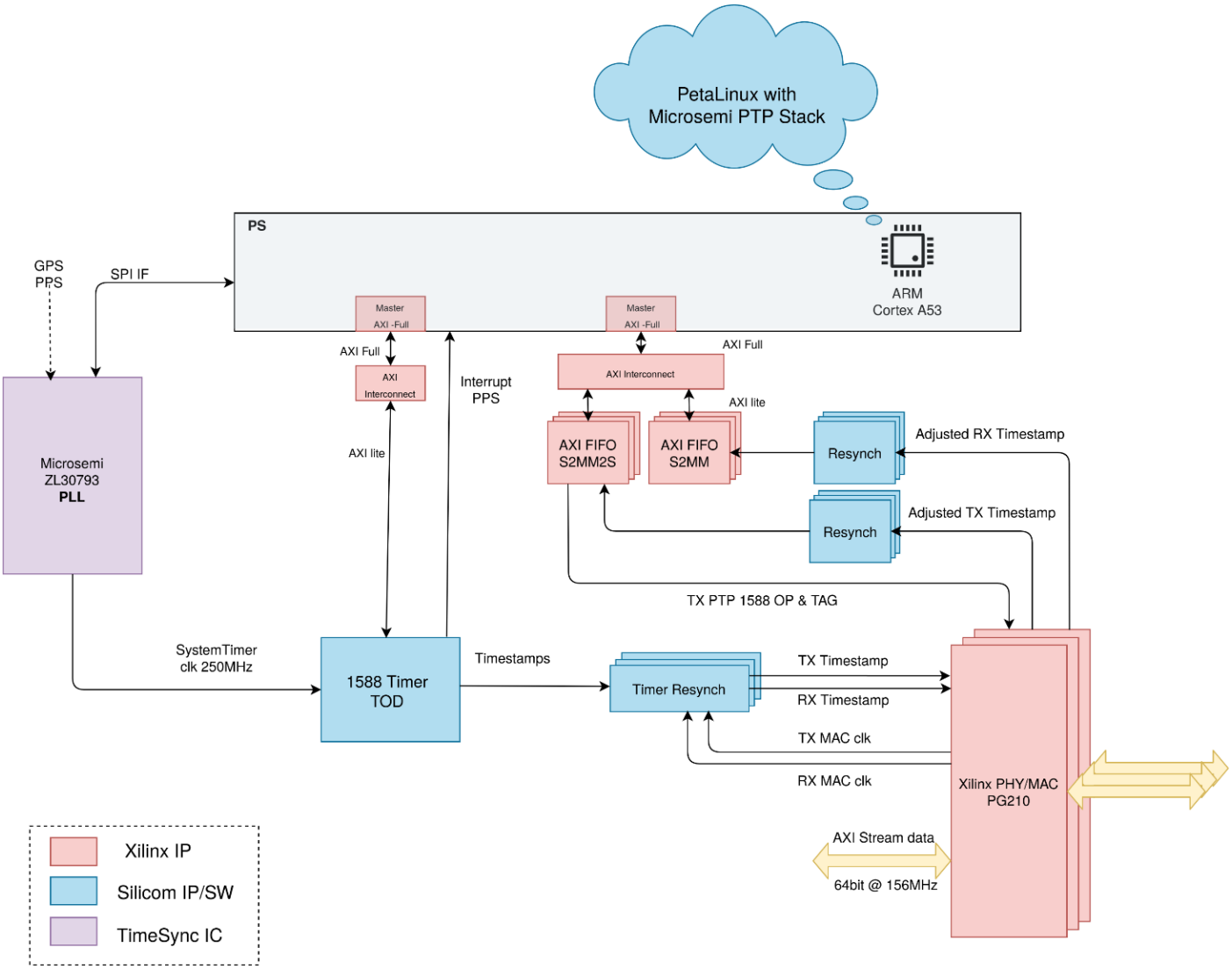
- ORAN LLS-C1 and C2
- Support 1588/PTP over IPv4 / IPV6, IEEE1588v2
- Support SyncE /ITU-T G.8262
- T-BC/T-TSC Boundary Clock and TSC Slave Clock /G.8273.2
- OC Own Clock (Master / Slave) – Class C (Stratum 3e)
- Support for Minimum 4Hours Hold Over
- Software 1588 Stack and Servo SW in ARM



Description

1588 Hardware time stamping reference design on 4x10G front port configuration:

- Support for *ptp4l* on Petalinux using the hardware timestamping features
- Support for *phc2sys* on PetaLinux to sync the Cassino RTC from the PTP clock
- Support for *zlRegister* on PetaLinux for Microsemi PLL register access
- Xilinx 10G Ethernet MAC+PCS/PMA 64-bit, Base-R with two step Timestamping Logic enabled, *PG 210* v3.3
- *ToD* IP with *AXIL-4* interface, running on configurable clock frequency from the PLL.
- Timestamp synchronization from ToD clock to Ethernet clock domains



Cassino Ordering P/N

Product Family	Product Description	Ordering P/N
Cassino	FPGA PCIe card, 4xSFP28, ZU21DR FPGA SG-2, Clock reference, HW IEEE1588/PTP, 1xSMA GNSS, PCIe Gen3 X8,2x4GB DDR4, Passive cooling, full height, ½ Length	FB4XXVG@Z21D-2-LGP0
Cassino	FPGA PCIe card, 4xSFP28, ZU21DR FPGA SG-2, Clock reference, HW IEEE1588/PTP, 1xSMA PPS, PCIe Gen3 X8,2x4GB DDR4, Passive cooling, full height, ½ Length	FB4XXVG@Z21D-2-LPP0
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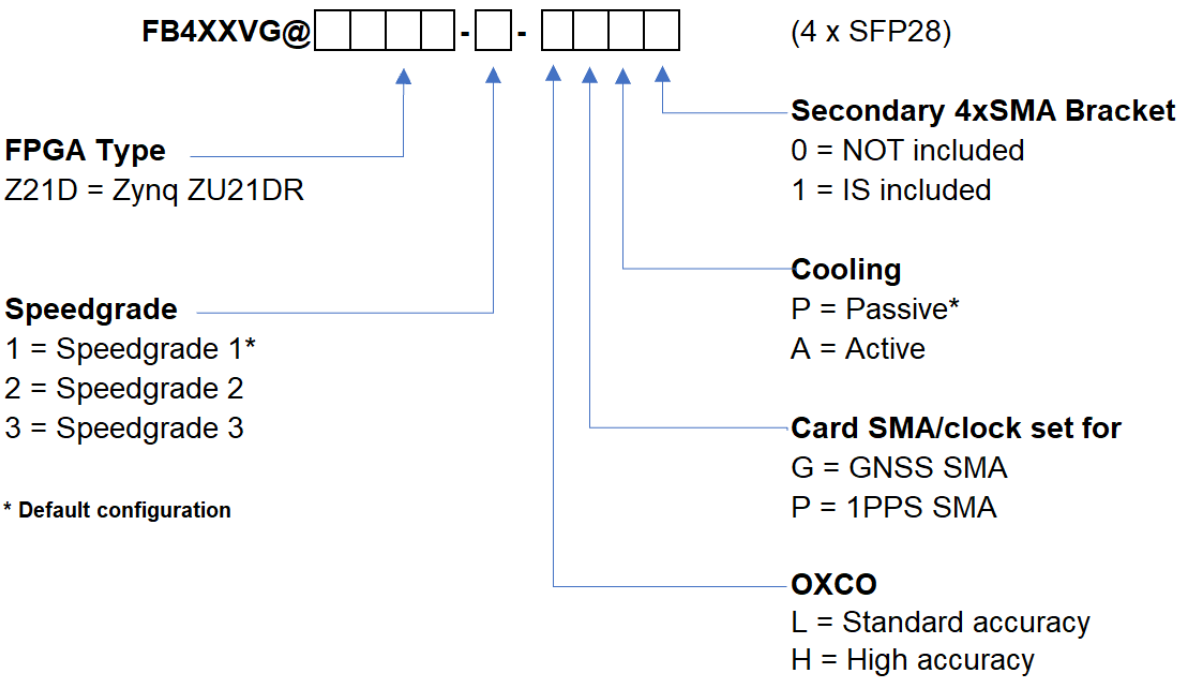
Cassino Product Ordering Guide



Cassino Release Plan

Delivery Date	Deliverable	Description
January 11th, 2021	First Customer Release	Version for 4x10G, network connectivity and xDMA server connectivity supplied Initial Hardware Design verification successfully completed
February 5th, 2021	First Customer IP porting complete	First release evaluation completed in collaboration with beta customers.
June 16th, 2021	Samples of revision 2 ready for shipment	Revision 2 hardware and upgraded board support package including FPGA reference design including 1588 “as-is” and PetaLinux 2020.2.
July 16th, 2021	General Availability revision 2	Pre-NEBS report completed. Available production volume limited due to component lead-times
September 30th, 2021	Start full volume production	

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