SNR-CFP4-ER4-40

Single-Mode 100GBASE 4WDM-40 CFP4 Transceiver
RoHS6 Compliant

Features

- Supports 103Gbps aggregate bit rates
- Single 3.3V Power Supply
- Up to 40km transmission on SMF with FEC
- Hot-Pluggable CFP4 Footprint Duplex LC Connector Interface
- Integrated High Performance EML TOSA and High Sensitivity APD ROSA
- Class 1 FDA and IEC60825-1 Laser Safety Compliant
- RoHS6 Compliant
- Operating Case Temperature
  Standard: 0℃~+70℃
- Compliant with CFP4 MSA Specification
- MDIO interface with integrated Digital Diagnostic Monitoring
- No external reference clock

Applications

- 100G Datacom & Telecom connections
- 100G 4WDM-40 40km applications with FEC

Ordering Information

Part No.	Data Rate	Distance*note2	Interface	Temp.	DDMI
SNR-CFP4-ER4-40*note1	103.125Gbps	40km	LC	Standard	Yes

Note1: Stand version
Note2: 9/125μm SMF
*The product image only for reference purpose.

Regulatory Compliance

Product Certificate	Certificate Number	Applicable Standard
TUV	R50135086	EN 60950-1:2006+A11+A1+A12+A2
		EN 60825-1:2014
		EN 60825-2:2004+A1+A2
UL	E317337	UL 60950-1
		CSA C22.2 No. 60950-1-07
EMC CE	AE 50384190 0001	EN 55032:2012
		EN 55032:2015
		EN 55024:2010
		EN 55024:2010+A1
'FCC	WTF14F0514417E	47 CFR PART 15 OCT., 2013
FDA	/	CDRH 1040.10
ROHS	/	2011/65/EU

Absolute Maximum Ratings*note4

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	Ts	-40	+85	°C
Supply Voltage	Vcc	-0.5	3.6	V
Operating Relative Humidity	RH	5	95	%

Note4: Exceeding any one of these values may destroy the device immediately.

Recommended Operating Conditions

Parameter	Symbol		Min.	Typical	Max.	Unit
Operating Case Temperature	T_C		0		70	°C
Power Supply Voltage	Vcc		3.2	3.3	3.4	V
Power Supply Noise	DC-1MHz			2		%
	1-10MHz			3		
Power Consumption	P	MAX			6	W
		Low Power Mode			1	
Time of Power-On sequence & Reset Sequence				TBD		sec
Modulation Format				NRZ, Mark Ratio 50%		

Performance Specifications - Electrical

Parameter	Symbol	Min.	Typ.	Max	Unit	Notes
Transmitter						
Input Amplitude (Differential)	Vin	150		1000	mVpp	AC coupled inputs*(Note6)
Input Impedance (Differential)	Zin	85	100	115	ohms	Rin > 100 kohms @ DC
Receiver						
Output Amplitude (Differential)	Vout	360		900	mVpp	AC coupled outputs*(Note6)
Output Impedance (Differential)	Zout	85	100	115	ohms	

1.2V MDIO Interface Specifications

Parameter	Symbol	Min.	Typ.	Max	Unit	Notes
Input Voltage	V_{IH}	0.84		1.5	V	
	V_{IL}	-0.3		0.36	V	
Input Leak current	I_{IN}	-100		100	uA	
Output Voltage	V_{OH}	1.0		1.5	V	
	V_{OL}	-0.3		0.2	V	
Input Capacitance	C_I			10	pF	
Input MDC Clock	f_{MDC}	0.1		4	MHz	
MDC Clock Period	T_{MDC}	250		10000	ns	
MDIO Hold Time	T_{hold}	10			ns	
MDIO SetupTime	T_{setup}	10			ns	
Clock to output delay from the MMD	T_{dely}	0		300	ns	
GLB_ALM	$T_{glb\_alm\_ass}$			150	ms	
	$T_{glb\_alm\_dea}$			150	ms	
MDC High time	T_{high}			160	ns	
MDC Low time	T_{low}			160	ns	

Optical and Electrical Characteristics

100GBASE-4WDM Operation

Parameter	Symbol	Min.	Typical	Max.	Unit
Transmitter					
Signaling Speed per Lane	BR_{AVE}		25.78		Gbps
Data Rate Variation		-100		+100	ppm
Lane_0 Center Wavelength	λ_{C0}	1294.53	1295.56	1296.59	nm
Lane_1 Center Wavelength	λ_{C1}	1299.02	1300.05	1301.09	nm
Lane_2 Center Wavelength	λ_{C2}	1303.54	1304.58	1305.63	nm
Lane_3 Center Wavelength	λ_{C3}	1308.09	1309.14	1310.19	nm
Total Average Output Power	Po			12.5	dBm
Average Launch Power per Lane	Peach	-2.5		6.5	dBm
Optical Modulation Amplitude per Lane		0.5		6.5	dBm
Average launch power of OFF transmitter per lane				-30	dBm
Optical Return Loss Tolerance				20	dB
Extinction Ratio	ER	4.5			dB
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}			
TX Disable Assert Time	t_off			100	us
Receiver					
Signaling Speed per Lane	BR_{AVE}		25.78		Gbps
Data Rate Variation		-100		+100	ppm
Damage threshold	Rdam	-2.5			dBm
Lane_0 Center Wavelength	λ_{C0}	1294.53	1295.56	1296.59	nm
Lane_1 Center Wavelength	λ_{C1}	1299.02	1300.05	1301.09	nm
Lane_2 Center Wavelength	λ_{C2}	1303.54	1304.58	1305.63	nm
Lane_3 Center Wavelength	λ_{C3}	1308.09	1309.14	1310.19	nm
Average Receive Power	Rpow	-20.5		TBD	dBm
Receive Sensitivity in OMA per Lane	Pmin			-18.5	dBm
LOS Assert	LOSA	-30			dBm
LOS De-Assert	LOSD			-20	dBm
LOS Hysteresis		0.5			dB

MDIO Registers for MCLK

MDIO Hex Addr	Access Type	Bit	Register Name	Value and Description	Notes
A011h	R/W	7:5	TX MCLK Control	000b: Disabled (Initial Value) 010b: 1/8 of network lane	
A012h	R/W	7:5	RX MCLK Control	000b: Disabled (Initial Value) 010b: 1/8 of network lane	
A015h	R/W	13:12	MCLK Selection	Selects the source of the MCLK for CFP4 modules. 00b: MCLK Off (Initial Value). 01b: MCLK = TX_MCLK 10b: Reserved. 11b: Reserved.	

MDIO Registers for Host Lane Control Controls Selection

MDIO Hex Addr	Access Type	Bit	Register Name	Value and Description	Notes
A440~A443h	R/W	15	Signal equalization mode control	0: Automatic (Initial Value) 1: Manual	
	R/W	12~9	Signal Equalization Gain	00h: No EQ (Initial Value). Write 9~0 to set 9 ~ 0 Db of gain in manual mode.	
	R/W	3~0	Rx Signal Pre/ De-emphasis	0000b: 0dB (Initial Value). 4-bit unsigned number N represents the pre/de-emphasis applied. Pre/De-emphasis = 0.5 dB * N, N = 0, 15.	

MDIO Registers for Host Lane RX Squelch Mode Selection

MDIO Hex Addr	Access Type	Bit	Register Name	Value and Description	Notes
A014h	R/W	9	Automatic Host Lane Output Squelch on LOS	0: Host Lane shall not squelch Rx RF output on RX_LOS. Host controls squelch using A040h (Initial Value). 1: Host Lane shall squelch Rx RF output on RX_LOS (sync with A210h~A21Fh.4) per lane based.	
A040h	R/W	15~0	Host Lane Output Squelch Control	Bits 15~0 squelches host lane 15~0 Rx RF output respectively. 0: No squelch(Initial Value). 1: Squelch.	

MDIO Registers for Network Lane Squelch & Disable Selection

MDIO Hex Addr	Access Type	Bit	Register Name	Value and Description	Notes
A011h	R/W	15	Automatic Network Lane TX Squelch Mode	0: Network Lane shall squelch TX Average power on TX_LOL (sync with A210h~A21Fh.6) per lane base (Initial Value). 1: Network Lane shall squelch TX OMA power on TX_LOL (sync with A210h~A21Fh.6) per lane base.	
	R/W	4	Automatic Network Lane TX Squelch Control	0: Network lane automatic control on TX_LOL is off. Host controls each lane TX squelch using A041h (Initial Value). 1: Network lane automatic control on TX_LOL is on per lane base.	
A013h	R/W	15~0	Lane 15~0 Disable	Bits 15~0 disable network lane 15~0 Tx Average power output respectively. 0: Normal(Initial Value). 1: Disable.	
A041h	R/W	15~0	Network Lane n TX Squelch	Bits 15~0 squelches network lane 15~0 Tx OMA power output respectively. 0: No squelch(Initial Value). 1: Squelch.	

MDIO Registers for TX/Rx Reset

MDIO Hex Addr	Access Type	Bit	Register Name	Value and Description	Notes
A011h	R/W	8	TX Reset	0: Normal operation(Initial Value), 1: Reset.	Note15
A012h	R/W	8	RX Reset	0: Normal operation(Initial Value), 1: Reset.	Note15

Note15: Set these registers to 1 will keep the correspond CDR in reset sate. While these bits are cleared, the correspond CDR will be re-initialized.

MDIO Registers for PRG_CNTL1/Tx_DIS

MDIO Hex Addr	Access Type	Bit	Register Name	Value and Description	Notes
A007h	R/W	7~0	Function Select Code	0: Assert/De-Assert of PRG_CNTL1 has no effect. 0x01: Assign TRXIC_RSTn function to hardware pins PRG_CNTL1. When so assigned this pin uses the active low logic, that is, 0 =Assert (Reset). 2~9: MSA reserved. 0x0A: TX_DIS (Initial Value).	Note14

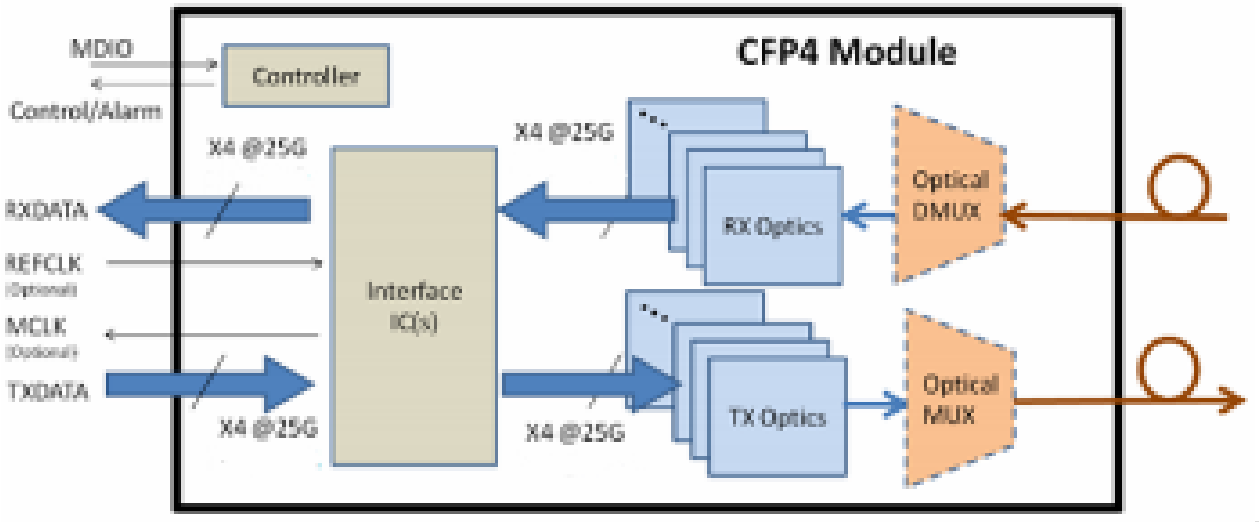
Note14: CFP4 module multiplexes PRG_CNTL1 with TX_DIS functions. Host shall use this register to assign TX_DIS function to PRG_CNTL1,if and only if module is in Low_Power State. When A007h is set to 0x01 in low power state, then the TRXIC_RSTn function is enabled and the hardware TX_DIS is assigned to be deasserted.

MDIO Registers for PRG_ALRM1

MDIO Hex Addr	Access Type	Bit	Register Name	Value and Description	Notes
A00Ah	R/W	7~0	Alarm Source Code	0: Not active, always de-asserted, 1: HIPWR_ON, MSA default setting, 2: Ready State, 3: Fault State, 4: RX_ALRM = RX_LOS + RX_NETWORK_LOL, 5: TX_ALRM = TX_LOSF + TX_HOST_LOL + TX_CMU_LOL, 6: RX_NETWORK_LOL, 7: TX_LOSF, 8: TX_HOST_LOL, 9: OOA, 10: RX_LOS(Initial Value). 11~255: Reserved.	

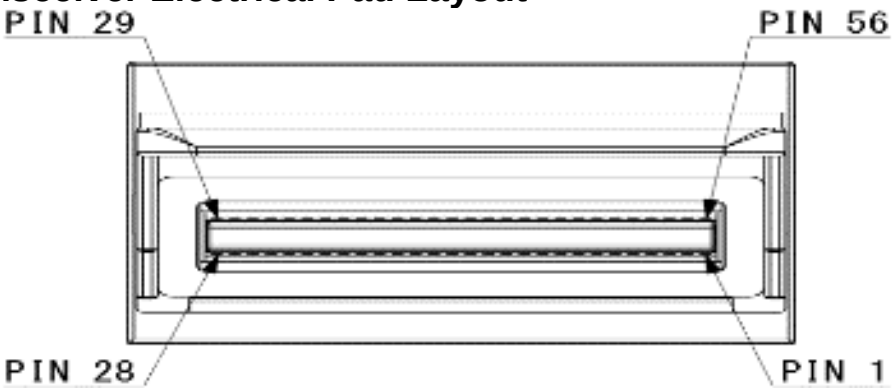
MDIO Registers for RX Power Monitor Alarm/Warning Threshold

MDIO Hex Addr	Access Type	Bit	Register Name	Value and Description	Notes
A015h	R/W	9	RX Power Monitor Alarm/Warning Threshold Select	0: MSA default registers 80C0h~80C7h (Initial Value), 1: Host Configured Receive Optical Power Threshold registers A03Ch~A03Fh..	Note15
A03Ch	R/W	15~0	Host Configured Receive Optical Power High Alarm Threshold	Valid if the value is between “Host Configured Receive Optical Power High Alarm Permissible Minimum Threshold” (80E8h) and “Host Configured Receive Optical Power High Alarm Permissible Maximum Threshold” (80F0h). Value beyond the threshold shall generate no effect.	
A03Dh	R/W	15~0	Host Configured Receive Optical Power High Warning Threshold	Valid if the value is between “Host Configured Optical Power High Warning Permissible Minimum Threshold” (0x80EA) and “Host Configured Optical Power High Warning Permissible Maximum Threshold” (80F2h). Value beyond the threshold shall generate no effect.	
A03Eh	R/W	15~0	Host Configured Receive Optical Power Low Warning Threshold	Valid if the value is between “Host Configured Optical Power Low Warning Permissible Minimum Threshold” (80Ech) and “Host Configured Optical Power Low Warning Permissible Maximum Threshold” (80F4h). Value beyond the threshold shall generate no effect.	
A03Fh	R/W	15~0	Host Configured Receive Optical Power Low Alarm Threshold	Valid if the value is between “Host Configured Receive Optical Power Low Alarm Permissible Minimum Threshold” (80Eeh) and “Host Configured Receive Optical Power Low Alarm Permissible Maximum Threshold” (80F6h). Value beyond the threshold shall generate no effect.	



Functional Description of Transceiver

CFP4 Transceiver Electrical Pad Layout



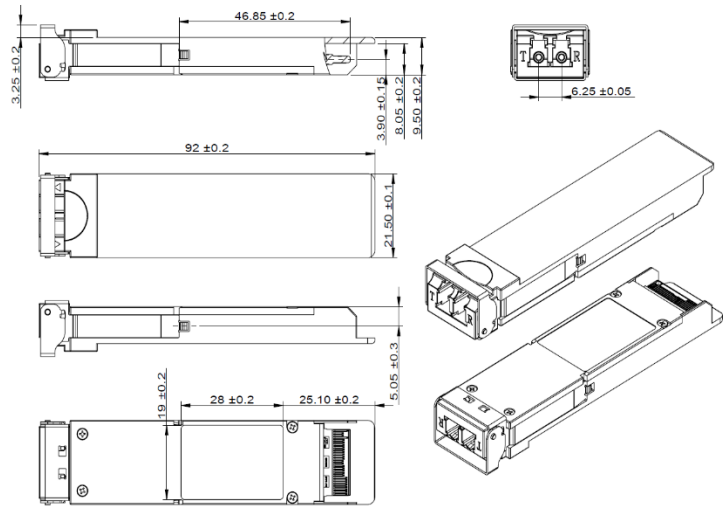
Pin Function Definitions

CFP4 Top	
56	GND
55	TX3n
54	TX3p
53	GND
52	TX2n
51	TX2p
50	GND
49	TX1n
48	TX1p
47	GND
46	TX0n
45	TX0p
44	GND
43	*(REFCLKn)*
42	*(REFCLKp)*
41	GND
40	RX3n
39	RX3p
38	GND
37	RX2n
36	RX2p
35	GND
34	RX1n
33	RX1p
32	GND
31	RX0n
30	RX0p
29	GND

CFP4 Bottom	
1	3.3V_GND
2	3.3V_GND
3	3.3V
4	3.3V
5	3.3V
6	3.3V
7	3.3V_GND
8	3.3V_GND
9	VND_IO_A
10	VND_IO_A
11	TX_DIS (PRG_CNTL1)
12	RX_LOS (PRG_ALRM1)
13	GLB_ALRMn
14	MOD_LOPWR
15	MOD_ABS
16	MOD_RSTn
17	MDC
18	MDIO
19	PRTADR0
20	PRTADR1
21	PRTADR2
22	VND_IO_C
23	VND_IO_D
24	VND_IO_E
25	GND
26	*(MCLKn)*
27	*(MCLKp)*
28	GND

Mechanical Specifications

Parameter	Symbol	Max.	Unit	Spec
Weight		90	g	
Flatness		0.12	mm	CFP MSA CFP4 HW spec Rev.0.1_5.3.1=0.12mm(class=4)
Roughness	Ra	1.6	μ m	CFP MSA CFP4 HW spec Rev.0.1_5.3.1=0.16mm(class=4)



LC Connector

GUARANTEE:

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