SFF Committee

SFF-8472 Specification for

Diagnostic Monitoring Interface for Optical Transceivers

Rev 11.0 September 13, 2010

Secretariat: SFF Committee

Abstract: This specification defines an enhanced digital diagnostic monitoring interface for optical transceivers which allows real time access to device operating parameters.

This specification provides a common reference for systems manufacturers, system integrators, and suppliers. This is an internal working specification of the SFF Committee, an industry ad hoc group.

This specification is made available for public review, and written comments are solicited from readers. Comments received by the members will be considered for inclusion in future revisions of this specification.

Support: This specification is supported by the identified member companies of the SFF Committee.

POINTS OF CONTACT:

Technical Editor:
Randy Clark
Avago Technologies
350 West Trimble Rd
San Jose, CA, 95131
408-435-6763
randy.clark@avagotech.com

Chairman SFF Committee
I. Dal Allan
14426 Black Walnut Court
Saratoga
CA 95070
408-867-6630
408-867-2115Fx
endlcom@acm.org

Technical Contributors:
Randy Clark, Agilent Technologies
Pete Mahowald, Agilent Technologies
Tom Lindsay, E2O
Lew Aronson, Finisar
Dan Kane, Finisar
Leland Day, JDS Uniphase
Jim Judkins, Micrel Semiconductor
Gus Carroll, Pine Photonics
Luis Torres, Stratos Lightwave

EXPRESSION OF SUPPORT BY MANUFACTURERS

The following member companies of the SFF Committee voted in favor of this industry specification.

AMCC	JDS Uniphase
Arista Networks	Luxtera
Avago	Madison Cable
Broadcom	Micrel
Clariphy	Molex
EMC	NetLogic uSyst
Emulex	Nexans
ENDL	OpNext
ETRI	Panduit
Finisar	Picolight
Hewlett Packard	Samsung
Hitachi GST	Stratos
Honda Connector	Sun Microsystems
IBM	Unisys
Infineon	Vitesse Semiconductor
Intel	W L Gore

The following member companies of the SFF Committee voted to abstain on this industry specification.

Adaptec	Hitachi Cable
Amphenol	LSI
Brocade	Maxtor
Comax	Montrose/CDT
Cortina Systems	Panasonic
DDK Fujikura	QLogic
Dell	Seagate
FCI	Sumitomo
Foxconn	Toshiba America
Fujitsu Components	Tyco
Fujitsu CPA	Volex
Hitachi America	Xyratex

The user's attention is called to the possibility that implementation to this Specification may require use of an invention covered by patent rights. By distribution of this Specification, no position is taken with respect to the validity of this claim or of any patent rights in connection therewith. The patent holder has filed a statement of willingness to grant a license under these rights on reasonable and non-discriminatory terms and conditions to applicants desiring to obtain such a license.

Foreword

The development work on this specification was done by the SFF Committee, an industry group. The membership of the committee since its formation in August 1990 has included a mix of companies which are leaders across the industry.

When 2 1/2" diameter disk drives were introduced, there was no commonality on external dimensions e.g. physical size, mounting locations, connector type, connector location, between vendors.

The first use of these disk drives was in specific applications such as laptop portable computers and system integrators worked individually with vendors to develop the packaging. The result was wide diversity, and incompatibility.

The problems faced by integrators, device suppliers, and component suppliers led to the formation of the SFF Committee as an industry ad hoc group to address the marketing and engineering considerations of the emerging new technology.

During the development of the form factor definitions, other activities were suggested because participants in the SFF Committee faced more problems than the physical form factors of disk drives. In November 1992, the charter was expanded to address any issues of general interest and concern to the storage industry. The SFF Committee became a forum for resolving industry issues that are either not addressed by the standards process or need an immediate solution.

Those companies which have agreed to support a specification are identified in the first pages of each SFF Specification. Industry consensus is not an essential requirement to publish an SFF Specification because it is recognized that in an emerging product area, there is room for more than one approach. By making the documentation on competing proposals available, an integrator can examine the alternatives available and select the product that is felt to be most suitable.

SFF Committee meetings are held during T10 weeks (see www.t10.org), and Specific Subject Working Groups are held at the convenience of the participants. Material presented at SFF Committee meetings becomes public domain, and there are no restrictions on the open mailing of material presented at committee meetings.

Most of the specifications developed by the SFF Committee have either been incorporated into standards or adopted as standards by EIA (Electronic Industries Association), ANSI (American National Standards Institute) and IEC (International Electrotechnical Commission).

If you are interested in participating or wish to follow the activities of the SFF Committee, the signup for membership and/or documentation can be found at:

www.sffcommittee.com/ie/join.html

The complete list of SFF Specifications which have been completed or are currently being worked on by the SFF Committee can be found at:

ftp://ftp.seagate.com/sff/SFF-8000.TXT

If you wish to know more about the SFF Committee, the principles which guide the activities can be found at:

ftp://ftp.seagate.com/sff/SFF-8032.TXT

Suggestions for improvement of this specification will be welcome. They should be sent to the SFF Committee, 14426 Black Walnut Ct, Saratoga, CA 95070.

Publication History

Revision Number	Description	Date
1.0	Initial Submission of Document, Preliminary	4/5/01
2.0	Draft Second Revision, Preliminary	5/18/01
3.0	Draft Third Revision, Preliminary	6/27/01
4.0	Draft Fourth Revision, Preliminary	10/8/01
5.0	Draft Fifth Revision	11/5/01
6.0	Draft Sixth Revision	11/19/01
7.0	Draft Revision 7.0	01/09/02
8.0	Draft Revision 8.0	02/01/02
9.0	Draft Revision 9.0	03/28/02
9.0	Revision 9.0 Approved for Technical Content	5/02
9.2	Revision 9.2 Submitted for Publication	5/30/02
9.3	Editorial Modifications to rev. 9.2. 9.3 Submitted for Publication	8/01/02
9.4	Add extensions to include additional technologies. Results of Dec. 5 03 discussions. Includes: Support for Multiple Application Selection Reserved values for SFF-8079 in Table 3.1, Table 3.10, Table 3.12, and Table 3.17. Additional transceiver type values in Table 3.5 Additional values in Table 3.1a, 3.5a and 3.5b Additional values in Table 3.12 General editorial modifications.	5/26/04
9.5	Editorial Modifications to rev. 9.4. 9.5 Submitted for Publication.	6/01/04
10.0	Add extensions to the following tables: Table 3.1b, 3.2, 3.4, 3.5, 3.5b, 3.7, 3.11, 3.12, 3.21 Editorial changes to the following tables: Table 3.2, 3.3, 3.4, 3.6, 3.7, 3.9, 3.10, 3.17 Add table 3.1a, 3.6a, 3.18a and references to 8079/8431.	2/06/07
10.2	Editorial updates per ballot feedback. Technical update to Tables 3.1.	6/01/07
10.3	Edits per SFF-8431	12/07/07
10.4	Edits per SFF-8431, add bits in Table 3.5 and add Tables 3.6b and 3.6c for SFF-8431 and SFF-8461. Add Table 3.1c.	1/30/09
10.5	Edits per FC-PI-5 (16GFC) to tables 3.6a,3.12,	5/21/10

Reference	Revision 9.3	Revision 9.4/9.5	Revision 10.2/10.4
Section 2 Applicable Documents	GBIC and SFP MSA	Add: SFF 8079 and 8089	Add SFF 8431
Table 3.1 Address A0h	Base definition	Byte 13 = Reserved for SFF-8079 Bytes 128-255 Reserved for SFF-8079	Byte 13 = Rate Identifier Byte 19 = OM3 Link Length Bytes 128-255 Reserved for SFF-8079
Table 3.1a	n/a	Add Transceiver ID Examples	Change to A2h Diagnostic Fields
Table 3.1b	n/a	n/a	Add Transceiver ID Examples
Table 3.1c	n/a	n/a	Add Transceiver ID Examples
Table 3.2 Identifiers	Same as SFP MSA 8074	Same as SFP MSA 8074	Add 04h to 0Ch for alternate MSAs
Table 3.4 Connectors	Same as SFP MSA 8074	Same as SFP MSA 8074	Add 0Ch and 22h for new connectors
Table 3.5 Transceiver Compliance	Add Sonet and IB to SFP MSA 8074	Add ESCON, EFM, Copper and 8G	Add 10GE, 10GFC, OC-192, FC Base-T and medium FC length
Table 3.5a Sonet Compliance	Base definition	Add short reach SR-1	<same>
Table 3.5b Transceiver ID Examples	n/a	Add Base definition	Add more examples
Table 3.6 Encoding	Same as SFP MSA 8074	Same as SFP MSA 8074	Add 06h = 64B/66B
Table 3.6a Rate Identifier	n/a	n/a	Add Base definition
Table 3.6b Cable Identifier	n/a	n/a	Add Base definition
Table 3.6c Cable Identifier	n/a	n/a	Add Base definition
Table 3.7 Option Values	Same as SFP MSA 8074	Same as SFP MSA 8074	Add Byte 64h for SFF 8431
Table 3.10 Enhanced Options	Base definition	Add Byte 93, Bit 2 for SFF 8079	Add Byte 93, Bit 1 for SFF-8431
Table 3.11 Soft Timing	Base definition	<same>	Add t_power_level2 for SFF-8431
Table 3.12 Compliance	01h = revision 9.3	Add 02h = revision 9.5	Add 03h = revision 10
Table 3.17 Status/Control	Base definition	Reserve 110h/5 and all of 111h for SFF 8079	Editorial changes only
Table 3.18 Alarm/Warning Flags	Base definition	<same>	Remove bytes 118 and 119 for Table 3.18a
Table 3.18a Extended Status/Control	n/a	n/a	Add Byte 118 for SFF 8431

Reference	Revision 10.4	Revision 10.5
Section 2 Applicable Documents	Add SFF 8431	<no change>
Table 3.1 Address A0h	Byte 13 = Rate Identifier Byte 19 = OM3 Link Length Bytes 128-255 Reserved for SFF-8079	<no change>
Table 3.1a	Change to A2h Diagnostic Fields	<no change>
Table 3.1b	Add Transceiver ID Examples	<no change>
Table 3.1c	Add Transceiver ID Examples	<no change>
Table 3.2 Identifiers	Add 04h to 0Ch for alternate MSAs	<no change>
Table 3.4 Connectors	Add 0Ch and 22h for new connectors	<no change>
Table 3.5 Transceiver Compliance	Add 10GE, 10GFC, OC-192, FC Base-T and medium FC length	<no change>
Table 3.5a Sonet Compliance	<same>	<no change>
Table 3.5b Transceiver ID Examples	Add more examples	<no change>
Table 3.6 Encoding	Add 06h = 64B/66B	<no change>
Table 3.6a Rate Identifier	Add Base definition	Expand to add 08h and 0Ah for FC-PI-5
Table 3.6b Cable Identifier	Add Base definition	<no change>
Table 3.6c Cable Identifier	Add Base definition	<no change>
Table 3.7 Option Values	Add Byte 64h for SFF 8431	<no change>
Table 3.10 Enhanced Options	Add Byte 93, Bit 1 for SFF-8431	<no change>
Table 3.11 Soft Timing	Add t_power_level2 for SFF-8431	<no change>
Table 3.12 Compliance	Add 03h = revision 10	Add 05h = revision 10.5
Table 3.17 Status/Control	Editorial changes only	<no change>
Table 3.18 Alarm/Warning Flags	Remove bytes 118 and 119 for Table 3.18a	<no change>
Table 3.18a Extended Status/Control	Add Byte 118 for SFF 8431	<no change>

1. Scope and Overview

This document defines an enhanced memory map with a digital diagnostic monitoring interface for optical transceivers that allows pseudo real time access to device operating parameters. It also adds new options to the previously defined two-wire interface ID memory map that accommodate new transceiver types that were not considered in the SFP MSA or GBIC documents.

The interface is an extension of the two-wire interface ID interface defined in the GBIC specification as well as the SFP MSA. Both specifications define a 256 byte memory map in EEPROM which is accessible over a 2 wire serial interface at the 8 bit address 1010000X (A0h). The digital diagnostic monitoring interface makes use of the 8 bit address 1010001X (A2h), so the originally defined two-wire interface ID memory map remains unchanged. The interface is backward compatible with both the GBIC specification and the SFP MSA.

2. Applicable Documents

Gigabit Interface Converter (GBIC). SFF document number: SFF-8053, rev. 5.5, September 27, 2000.

Small Form Factor Pluggable (SFP) Transceiver, SFF document number INF-8074, rev. 1.0, May 12, 2001 (Based on the initial September 14, 2001 MSA public release).

SFP Rate and Application Selection. SFF document number SFF-8079, rev 1.7, February 2, 2005.

SFP Rate and Application Codes. SFF document number SFF-8089, rev 1.3, February 3, 2005.

Enhanced 8.5 and 10 Gigabit Small Form Factor Pluggable Module (SFP Plus).
SFF document number SFF-8431, rev 1.6, December 21, 2006.

3. Enhanced Digital Diagnostic Interface Definition

Overview

The enhanced digital diagnostic interface is a superset of the MOD_DEF interface defined in the SFP MSA document dated September 14, 2000, later submitted to the SFF Committee as INF-8074. The 2 wire interface pin definitions, hardware, and timing are clearly defined there.

This document describes an extension to the memory map defined in the SFP MSA (see Figure 3.1). The enhanced interface uses the two wire serial bus address 1010001X (A2h) to provide diagnostic information about the module's present operating conditions. The transceiver generates this diagnostic data by digitization of internal analog signals. Calibration and alarm/warning threshold data is written during device manufacture.

All bits that are unallocated or reserved for SFF-8472 shall be set to zero and/or ignored.
Bits labeled as reserved or optional for other usage, such as for SFF-8079, shall be implemented per such other documents, or set to zero and/or ignored if not implemented.

If optional features for SFF-8472 are implemented, they shall be implemented as defined in SFF-8472. If they are not implemented, then write bits will be ignored, and state bits shall be set to zero.

Additional A0h and A2h memory allocations were provided in revision 9.5 to support multi-rate and application selection as defined in SFF-8079 and SFF-8089 documents.

Extensions have been made in revision 10.4 to several tables documenting new connectors, industry form factors and transceiver codes.

Figure 3.1: Digital Diagnostic Memory Map
Specific Data Field Descriptions

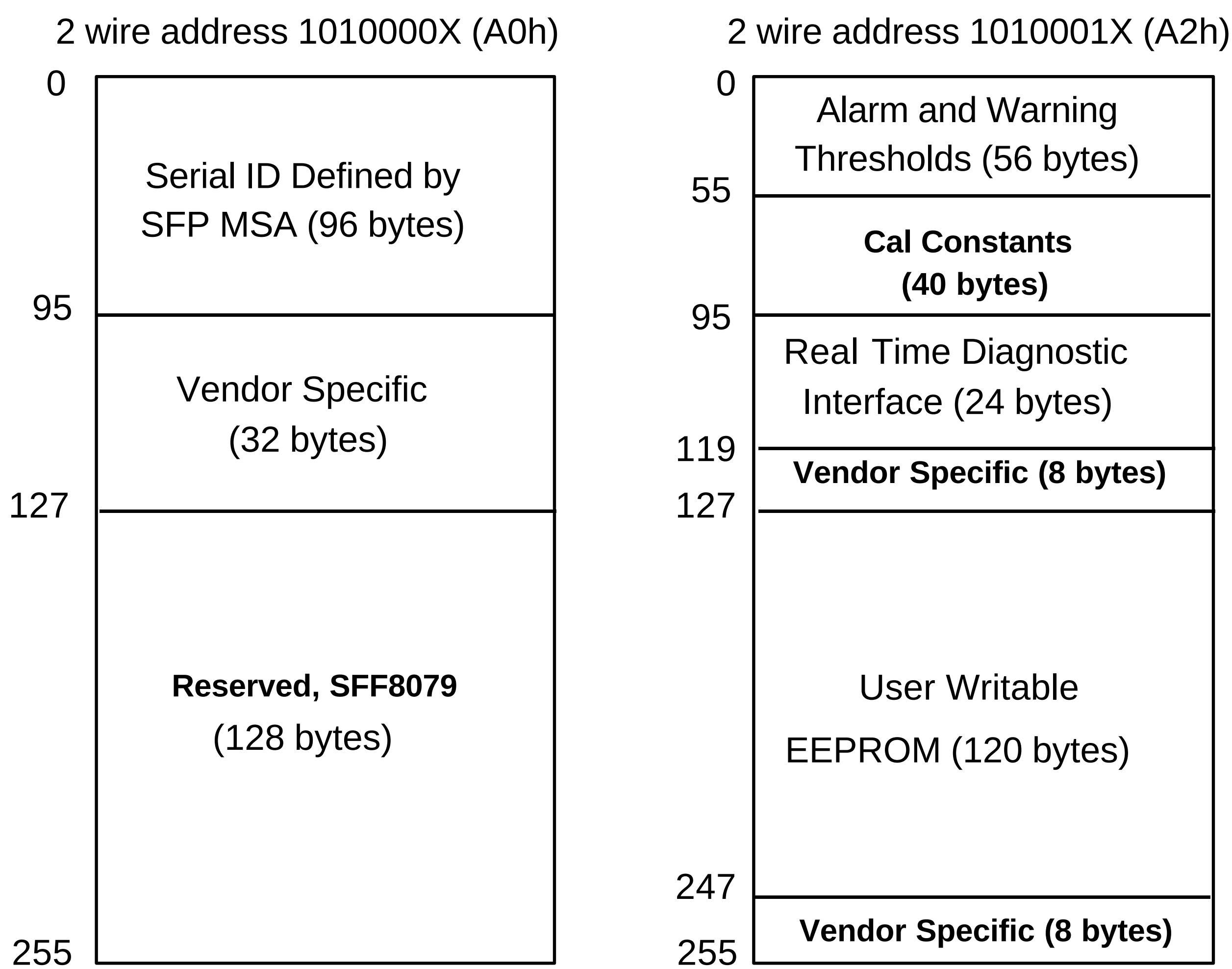

Table 3.1 Two-wire interface ID: Data Fields – Address A0h

Data Address	Size (Bytes)	Name of Field	Description of Field
BASE ID FIELDS			
0	1	Identifier	Type of transceiver (see Table 3.2)
1	1	Ext. Identifier	Extended identifier of type of transceiver (see Table 3.3)
2	1	Connector	Code for connector type (see Table 3.4)
3-10	8	Transceiver	Code for electronic or optical compatibility (see Table 3.5)
11	1	Encoding	Code for high speed serial encoding algorithm (see Table 3.6)
12	1	BR, Nominal	Nominal signalling rate, units of 100MBd.
13	1	Rate Identifier	Type of rate select functionality (see Table 3.6a)
14	1	Length(SMF,km)	Link length supported for single mode fiber, units of km
15	1	Length (SMF)	Link length supported for single mode fiber, units of 100 m
16	1	Length (50um)	Link length supported for 50 um OM2 fiber, units of 10 m
17	1	Length (62.5um)	Link length supported for 62.5 um OM1 fiber, units of 10 m
18	1	Length (cable)	Link length supported for copper or direct attach cable, units of m
19	1	Length (OM3)	Link length supported for 50 um OM3 fiber, units of 10 m
20-35	16	Vendor name	SFP vendor name (ASCII)
36	1	Transceiver	Code for electronic or optical compatibility (see Table 3.5)
37-39	3	Vendor OUI	SFP vendor IEEE company ID
40-55	16	Vendor PN	Part number provided by SFP vendor (ASCII)
56-59	4	Vendor rev	Revision level for part number provided by vendor (ASCII)
60-61	2	Wavelength	Laser wavelength (Passive/Active Cable Specification Compliance)
62	1	Unallocated	
63	1	CC_BASE	Check code for Base ID Fields (addresses 0 to 62)
EXTENDED ID FIELDS			
64-65	2	Options	Indicates which optional transceiver signals are implemented (see Table 3.7)
66	1	BR, max	Upper bit rate margin, units of %
67	1	BR, min	Lower bit rate margin, units of %
68-83	16	Vendor SN	Serial number provided by vendor (ASCII)
84-91	8	Date code	Vendor's manufacturing date code (see Table 3.8)
92	1	Diagnostic Monitoring Type	Indicates which type of diagnostic monitoring is implemented (if any) in the transceiver (see Table 3.9)
93	1	Enhanced Options	Indicates which optional enhanced features are implemented (if any) in the transceiver (see Table 3.10)
94	1	SFF-8472 Compliance	Indicates which revision of SFF-8472 the transceiver complies with. (see Table 3.12)
95	1	CC_EXT	Check code for the Extended ID Fields (addresses 64 to 94)
VENDOR SPECIFIC ID FIELDS			
96-127	32	Vendor Specific	Vendor Specific EEPROM
128-255	128	Reserved	Reserved for SFF-8079

Table 3.1a Diagnostics: Data Fields – Address A2h

Data Address	Size (Bytes)	Name of Field	Description of Field
DIAGNOSTIC AND CONTROL/STATUS FIELDS			
0-39	40	A/W Thresholds	Diagnostic Flag Alarm and Warning Thresholds (see Table 3.15)
40-55	16	Unallocated	
56-91	36	Ext Cal Constants	Diagnostic calibration constants for optional External Calibration (see Table 3.16)
92-94	3	Unallocated	
95	1	CC_DMI	Check code for Base Diagnostic Fields (addresses 0 to 94)
96-105	10	Diagnostics	Diagnostic Monitor Data (internally or externally calibrated) (see Table 3.17)
106-109	4	Unallocated	
110	1	Status/Control	Optional Status and Control Bits (see Table 3.17)
111	1	Reserved	Reserved for SFF-8079
112-113	2	Alarm Flags	Diagnostic Alarm Flag Status Bits (see Table 3.18)
114-115	2	Unallocated	
116-117	2	Warning Flags	Diagnostic Warning Flag Status Bits (see Table 3.18)
118-119	2	Ext Status/Control	Extended module control and status bytes (see Table 3.18a)
GENERAL USE FIELDS			
120-127	8	Vendor Specific	Vendor specific memory addresses (see Table 3.19)
128-247	120	User EEPROM	User writable non-volatile memory (see Table 3.20)
248-255	8	Vendor Control	Vendor specific control addresses (see Table 3.21)

Examples of transceiver and copper cable performance codes are given in Table 3.1b and Table 3.1c for illustration. Compliance to additional standards and technologies is possible so bits other than those indicated in each row may also be set to indicate compliance to these additional standards and technologies.

Table 3.1b: Transceiver Identification/Performance Examples (A0h Bytes 12-18)

		Address A0h Rate and Distance Fields						Wavelength Fields
Transceiver Type	**Transceiver Description**	**Byte 12**	**Byte 14**	**Byte 15**	**Byte 16**	**Byte 17**	**Byte 18**	**Bytes 60 & 61**
100-M5-SN-I and 100-M6-SN-I	1062.5 MBd MM 850nm 500m/50um, 300m/62.5um	0Bh	00h	00h	32h	1Eh	00h	0352h
200-SM-LC-L and 100-SM-LC-L	2125 MBd and 1062.5 MBd 10km SM 1310nm	15h[3]	0Ah[3]	64h[3]	00h	00h	00h	051Eh
400-M5-SN-I and 400-M6-SN-I [4]	4250 MBd MM 850nm 150m/50um, 70m/62.5um	2Bh[3]	00h	00h	0Fh[3]	07h[3]	00h	0352h
400-SM-LC-M	4250 MBd SM 1310nm 4km “medium” length	2Bh[3]	04h	28h	00h	00h	00h	051Eh
400-SM-LC-L	4250 MBd SM 1310nm 10km “long” length	2Bh[3]	0Ah	64h	00h	00h	00h	051Eh
200-SM-LL-V and 100-SM-LL-V	2125 MBd and 1062.5 MBd 50km SM 1550nm	15h[3]	32h	FFh	00h	00h	00h	060Eh
ESCON SM	200 MBd 20km SM 1310nm	02h	14h	C8h	00h	00h	00h	051Eh
100BASE-LX10	125 MBd 10km SM 1310nm	01h	0Ah	64h	00h	00h	00h	051Eh
1000BASE-T	1250 MBd 100m Cat 5 Cable	0Dh[1]	00h	00h	00h	00h	64h	0000h
1000BASE-SX	1250 MBd 550m MM 850nm	0Dh[1]	00h	00h	37h[2]	1Bh[2]	00h	0352h
1000BASE-LX	1250 MBd 5km SM 1310nm	0Dh[1]	05h	32h	37h	37h	00h	051Eh
1000BASE-LX10	1250 MBd 10km SM 1310nm	0Dh[1]	0Ah	64h	00h	00h	00h	051Eh
1000BASE-BX10-D	1250 MBd 10km SM 1490nm downstream TX	0Dh[1]	0Ah	64h	00h	00h	00h	05D2h
1000BASE-BX10-U	1250 MBd 10km SM 1310nm upstream TX	0Dh[1]	0Ah	64h	00h	00h	00h	051Eh
OC3/STM1 SR-1	155 MBd 2km SM 1310nm	02h	02h	14h	00h	00h	00h	051Eh
OC12/STM4 LR-1	622 MBd 40km SM 1310nm	06h[3]	28h	FFh	00h	00h	00h	051Eh
OC48/STM16 LR-2	2488 MBd 80km SM 1550nm	19h[3]	50h	FFh	00h	00h	00h	060Eh

1. By convention 1.25 Gb/s should be rounded up to 0Dh (13 in units of 100 MBd) for Ethernet 1000BASE-X.
2. Link distances for 1000BASE-SX variants vary between high and low bandwidth cable types per 802.3 Clause 38. The values shown are 270m [275m per 802.3] for 62.5um/200 MHz*km cable and 550m for 50um/500 MHz*km cable.
3. For transceivers supporting multiple data rates (and hence multiple distances with a single fiber type) the highest data rate and the distances achievable at that data rate are to be identified in these fields.
4. In this example, the transceiver supports 400-M5-SN-I, 200-M5-SN-I, 100-M5-SN-I, 400-M6-SN-I, 200-M6-SN-I and 100-M6-SN-I.

Table 3.1c: Copper Cable Identification/Performance Examples (A0h Bytes 7, 8, 60, 61)

	Link Length and Transmitter Technology		Laser wavelength and Cable Specification Compliance
Cable Type	**Byte 7**	**Byte 8**	**Bytes 60 and 61**
Passive Cable compliant to SFF-8431 Appendix E.	00h	04h	0100h
Active cable compliant to SFF-8431 Appendix E	00h	08h	0100h
Active cable compliant to SFF-8431 limiting	00h	08h	0400h
Active cable compliant to both SFF-8431 limiting and FC-PI-4 limiting	00h	08h	0C00h

Identifier [Address A0h, Byte 0]

The identifier value specifies the physical device described by two-wire interface information. This value shall be included in the two-wire interface data. The defined identifier values are shown in Table 3.2.

TABLE 3.2: Identifier values

A0h data address	Value	Description of physical device
0	00h	Unknown or unspecified
	01h	GBIC
	02h	Module soldered to motherboard (ex: SFF)
	03h	SFP or SFP “Plus”
	04h	Reserved for “300 pin XBI” devices*
	05h	Reserved for “Xenpak” devices*
	06h	Reserved for “XFP” devices*
	07h	Reserved for “XFF” devices*
	08h	Reserved for “XFP-E” devices*
	09h	Reserved for “XPak” devices*
	0Ah	Reserved for “X2” devices*
	0Bh	Reserved for “DWDM-SFP” devices*
	0Ch	Reserved for “QSFP” devices*
	0D-7Fh	Reserved, unallocated
	80-FFh	Vendor specific

* These device types are not impacted by this document and are shown only to avoid multiple industry definitions in this type of “Physical Device” identifier field.

Extended Identifier [Address A0h, Byte 1]

The extended identifier value provides additional information about the transceiver. The field should be set to 04h for all SFP modules indicating two-wire interface ID module definition. In many cases, a GBIC elects to use MOD_DEF 4 to make additional information about the GBIC available, even though the GBIC is actually compliant with one of the six other MOD_DEF values defined for GBICs. The extended identifier allows the GBIC to explicitly specify such compliance without requiring the MOD_DEF value to be inferred from the other information provided. The defined extended identifier values are shown in Table 3.3.

TABLE 3.3: Extended identifier values

A0h Data Address	Value	Description of connector
1	00h	GBIC definition is not specified or the GBIC definition is not compliant with a defined MOD_DEF. See product specification for details.
	01h	GBIC is compliant with MOD_DEF 1
	02h	GBIC is compliant with MOD_DEF 2
	03h	GBIC is compliant with MOD_DEF 3
	04h	GBIC/SFP function is defined by two-wire interface ID only
	05h	GBIC is compliant with MOD_DEF 5
	06h	GBIC is compliant with MOD_DEF 6
	07h	GBIC is compliant with MOD_DEF 7
	08-FFh	Unallocated

Connector [Address A0h, Byte 2]

The connector value indicates the external optical or electrical cable connector provided as the media interface. This value shall be included in the two-wire interface data. The defined connector values are shown in Table 3.4. Note that 01h to 05h are not SFP compatible, and are included for compatibility with GBIC standards.

TABLE 3.4: Connector values

A0h data address	Value	Description of connector
2	00h	Unknown or unspecified
	01h	SC
	02h	Fibre Channel Style 1 copper connector
	03h	Fibre Channel Style 2 copper connector
	04h	BNC/TNC
	05h	Fibre Channel coaxial headers
	06h	FiberJack
	07h	LC
	08h	MT-RJ
	09h	MU
	0Ah	SG
	0Bh	Optical pigtail
	0Ch	MPO Parallel Optic
	0D-1Fh	Unallocated
	20h	HSSDC II
	21h	Copper pigtail
	22h	RJ45
	23h-7Fh	Unallocated
	80-FFh	Vendor specific

Transceiver Compliance Codes [Address A0h, Bytes 3-10]

The following bit significant indicators define the electronic or optical interfaces that are supported by the transceiver. At least one bit shall be set in this field. For Fibre Channel transceivers, the Fibre Channel speed, transmission media, transmitter technology, and distance capability shall all be indicated. SONET compliance codes are completed by including the contents of Table 3.5a. Ethernet, ESCON and InfiniBand codes have been included to broaden the available applications of SFP transceivers.

Table 3.5: Transceiver codes(Address A0h)

Data Addr	Bit [1]	Description of transceiver	Data Addr	Bit [1]	Description of transceiver
Unallocated					
36	1-7	Unallocated			
10G Ethernet Compliance Codes			**Fibre Channel Link Length**		
36	0	Unallocated	7	7	very long distance (V)
3	7	10G Base-ER	7	6	short distance (S)
3	6	10G Base-LRM	7	5	intermediate distance (I)
3	5	10G Base-LR	7	4	long distance (L)
3	4	10G Base-SR	7	3	medium distance (M)
Infiniband Compliance Codes			**Fibre Channel Technology**		
3	3	1X SX	7	2	Shortwave laser, linear Rx (SA) [7]
3	2	1X LX	7	1	Longwave laser (LC) [6]
3	1	1X Copper Active	7	0	Electrical inter-enclosure (EL)
3	0	1X Copper Passive	8	7	Electrical intra-enclosure (EL)
ESCON Compliance Codes			8	6	Shortwave laser w/o OFC (SN) [7]
4	7	ESCON MMF, 1310nm LED	8	5	Shortwave laser with OFC [4] (SL)
4	6	ESCON SMF, 1310nm Laser	8	4	Longwave laser (LL) [5]
SONET Compliance Codes			**SFP+ Cable Technology**		
4	5	OC-192, short reach [2]	8	3	Active Cable [8]
4	4	SONET reach specifier bit 1	8	2	Passive Cable [8]
4	3	SONET reach specifier bit 2	**Unallocated**		
4	2	OC-48, long reach [2]	8	1	Unallocated
4	1	OC-48, intermediate reach [2]	8	0	Unallocated
4	0	OC-48, short reach [2]	**Fibre Channel Transmission Media**		
5	7	Unallocated	9	7	Twin Axial Pair (TW)
5	6	OC-12, single mode, long reach [2]	9	6	Twisted Pair (TP)
5	5	OC-12, single mode, inter. reach [2]	9	5	Miniature Coax (MI)
5	4	OC-12, short reach [2]	9	4	Video Coax (TV)
5	3	Unallocated	9	3	Multimode, 62.5um (M6)
5	2	OC-3, single mode, long reach [2]	9	2	Multimode, 50um (M5, M5E)
5	1	OC-3, single mode, inter. reach [2]	9	1	Unallocated
5	0	OC-3, short reach [2]	9	0	Single Mode (SM)
Ethernet Compliance Codes			**Fibre Channel Speed**		
6	7	BASE-PX [3]	10	7	1200 MBytes/sec
6	6	BASE-BX10 [3]	10	6	800 MBytes/sec
6	5	100BASE-FX	10	5	1600 MBytes/sec
6	4	100BASE-LX/LX10	10	4	400 MBytes/sec
6	3	1000BASE-T	10	3	Unallocated
6	2	1000BASE-CX	10	2	200 MBytes/sec
6	1	1000BASE-LX [3]	10	1	Unallocated
6	0	1000BASE-SX	10	0	100 MBytes/sec

[1] Bit 7 is the high order bit and is transmitted first in each byte.
[2] SONET compliance codes require reach specifier bits 3 and 4 in Table 3.5a to completely specify transceiver capabilities.
[3] Ethernet LX, PX and BX compliance codes require the use of the Bit Rate, Nominal value (byte 12), link length values for single mode and two types of multimode fiber (Bytes 14-17) and wavelength value for the laser (Bytes 60 & 61) as specified in Table 3.1 to completely specify transceiver capabilities. See Tables 3.1a and 3.5b for examples of setting values for these parameters.
[4] Note: Open Fiber Control (OFC) is a legacy eye safety electrical interlock system implemented on Gigabit Link Module (GLM) type transceiver devices and is not considered relevant to SFP transceivers.
[5] Laser type “LL” (long length) is usually associated with 1550nm, narrow spectral width lasers capable of very long link lengths.
[6] Laser type “LC” (low cost) is usually associated with 1310nm lasers capable of medium to long link lengths.
[7] Classes SN and SA are mutually exclusive. Both are without OFC. SN has a limiting Rx output, SA has a linear Rx output, per FC-PI-4.
[8] Refer to bytes 60 and 61 for definitions of the application copper cable standard specification.

The SONET compliance code bits allow the host to determine with which specifications a SONET transceiver complies. For each bit rate defined in Table 3.5 (OC-3, OC-12, OC-48), SONET specifies short reach (SR), intermediate reach (IR), and long reach (LR) requirements. For each of the three bit rates, a single short reach (SR) specification is defined. Two variations of intermediate reach (IR-1, IR-2) and three variations of long reach (LR-1, LR-2, and LR-3) are also defined for each bit rate. Byte 4, bits 0-2, and byte 5, bits 0-7 allow the user to determine which of the three reaches has been implemented – short, intermediate, or long. Two additional bits (byte 4, bits 3-4) are necessary to discriminate between different intermediate or long reach variations. These codes are defined in Table 3.5a.

Table 3.5a: SONET Compliance Specifiers (A0h)

Speed	Reach	Specifier bit 1 (Byte 4 bit 4)	Specifier bit 2 (Byte 4 bit 3)	Description
OC 3/OC 12/OC 48/OC 192	Short	0	0	SONET SR compliant [1]
OC 3/OC 12/OC 48/OC 192	Short	1	0	SONET SR-1 compliant [2]
OC 3/OC 12/OC 48	Intermediate	1	0	SONET IR-1 compliant
OC 3/OC 12/OC 48	Intermediate	0	1	SONET IR-2 compliant
OC 3/OC 12/OC 48	Long	1	0	SONET LR-1 compliant
OC 3/OC 12/OC 48	Long	0	1	SONET LR-2 compliant
OC 3/OC 12/OC 48	Long	1	1	SONET LR-3 compliant

[1] OC 3/OC 12 SR is multimode based short reach
[2] OC 3/OC 12 SR-1 is single-mode based short reach

Examples of transceiver code use are given in Table 3.5b for illustration.

Table 3.5b: Transceiver Identification Examples (A0h Bytes 3-10)

		Address A0h Transceiver Code Fields							
Transceiver Type	**Transceiver Description**	**Byte 3**	**Byte 4**	**Byte 5**	**Byte 6**	**Byte 7**	**Byte 8**	**Byte 9**	**Byte 10**
100-M5-SN-I and 100-M6-SN-I	1062.5 MBd MM 850nm 500m/50um, 300m/62.5um	00h	00h	00h	00h	20h	40h	0Ch	01h
200-SM-LC-L and 100-SM-LC-L	2125 MBd 10km SM 1310nm	00h	00h	00h	00h	12h	00h	01h	05h
400-M5-SN-I and 400-M6-SN-I [1]	4/2/1 GBd MM 850nm 150m/50um, 70m/62.5um	00h	00h	00h	00h	20h	40h	0Ch	15h
800-M5-SN-I and 800-M6-SN-I [1]	8/4/2 GBd MM 850nm 50um & 62.5um	00h	00h	00h	00h	20h	40h	0Ch	54h
400-SM-LC-M[1]	4250 MBd SM 1310nm 4km "medium" length	00h	00h	00h	00h	0Ah	00h	01h	15h
400-SM-LC-L[1]	4250 MBd SM 1310nm 10km "long" length	00h	00h	00h	00h	12h	00h	01h	15h
200-SM-LL-V and 100-SM-LL-V	2125 MBd 50km SM 1550nm	00h	00h	00h	00h	80h	10h	01h	05h
1000BASE-T	1250 MBd 100m Cat 5 Cable	00h	00h	00h	08h	00h	00h	00h	00h
1000BASE-SX	1250 MBd 550m MM 850nm	00h	00h	00h	01h	00h	00h	00h	00h
1000BASE-LX	1250 MBd 5km SM 1310nm	00h	00h	00h	02h[2]	00h	00h	00h	00h
1000BASE-LX10	1250 MBd 10km SM 1310nm	00h	00h	00h	02h[2]	00h	00h	00h	00h
10GBASE-SR	10.3125 GBd 300m OM3 MM 850nm	00h	00h	00h	00h	00h	00h	00h	20h
10GBASE-LR	10.3125 GBd 10km SM 1310nm	00h	00h	00h	00h	00h	00h	00h	10h
OC3/STM1 SR-1	155 MBd 2km SM 1310nm	00h	00h	01h	00h	00h	00h	00h	00h
OC12/STM4 LR-1	622 MBd 40km SM 1310nm	00h	10h	40h	00h	00h	00h	00h	00h
OC48/STM16 LR-2	2488 MBd 80km SM 1550nm	00h	0Ch	00h	00h	00h	00h	00h	00h
	10GE Passive copper cable with embedded SFP ends[3,4]	00h	00h	00h	00h	00h	04h	00h	00h
	10GE Active cable with embedded SFP ends[3,4]	00h	00h	00h	00h	00h	08h	00h	00h
	8/4/2G Passive copper cable with embedded SFP ends[3]	00h	00h	00h	00h	00h	04h	00h	54h
	8/4/2G Active cable with embedded SFP ends[3]	00h	00h	00h	00h	00h	08h	00h	54h

1. The assumption for this example is the transceiver is "4-2-1" compatible, meaning operational at 4.25 Gb/s, 2.125 Gb/s & 1.0625 Gb/s.
2. To distinguish between 1000BASE-LX and 1000BASE-LX10, A0h Bytes 12 to18 must be used … see Tables 3.1 and 3.1a for more information.
3. See A0h Bytes 60 and 61 for compliance of these media to industry electrical specifications.
4. For Ethernet and Sonet applications, data rate capability of these links will be identified in A0h Byte 12 [nominal bit rate identifier]. This is due to no formal IEEE designation for passive and active cable interconnects, and lack of corresponding identifiers in Table 3.5.

Encoding [Address A0h, Byte 11]

The encoding value indicates the serial encoding mechanism that is the nominal design target of the particular transceiver. For devices supporting multiple encoding types, the primary product application should dictate the value chose (ie. for 16G/8G/4G or 10G/1G, a value of 06h should be chosen). The value shall be contained in the two-wire interface data. The defined encoding values are shown in Table 3.6.

Table 3.6: Encoding codes

A0h data address	Value	Description of encoding mechanism
11	00h	Unspecified
	01h	8B/10B
	02h	4B/5B
	03h	NRZ
	04h	Manchester
	05h	SONET Scrambled
	06h	64B/66B
	07h -FFh	Unallocated

BR, nominal [Address A0h, Byte 12]

The nominal bit (signaling) rate (BR, nominal) is specified in units of 100 MBd, rounded off to the nearest 100 MBd. The bit rate includes those bits necessary to encode and delimit the signal as well as those bits carrying data information. A value of 0 indicates that the bit rate is not specified and must be determined from the transceiver technology. The actual information transfer rate will depend on the encoding of the data, as defined by the encoding value.

Rate Identifier [Address A0h, Byte 13]

The rate identifier byte refers to several (optional) industry standard definitions of Rate_Select or Application_Select control behaviors, intended to manage transceiver optimization for multiple operating rates.

Table 3.6a: Rate Identifier

A0h address	Value	Description of rate selection functionality
13	00h	Unspecified
	01h	Defined for SFF-8079 (4/2/1G Rate_Select & AS0/AS1)
	02h	Defined for SFF-8431 (8/4/2G Rx Rate_Select only)
	03h	Unspecified *
	04h	Defined for SFF-8431 (8/4/2G Tx Rate_Select only)
	05h	Unspecified *
	06h	Defined for SFF-8431 (8/4/2G Independent Rx & Tx Rate_select)
	07h	Unspecified *
	08h	Defined for FC-PI-5 (16/8/4G Rx Rate_select only) High=16G only, Low=8G/4G
	09h	Unspecified *
	0Ah	Defined for FC-PI-5 (16/8/4G Independent Rx, Tx Rate_select) High=16G only, Low=8G/4G
	0Bh -FFh	Unallocated

* To support legacy, the LSB is reserved for Unspecified or INF-8074 (value = 0) or 4/2/1G selection per SFF-8079 (value = 1). Other rate selection functionalities are not allowed to depend on the LSB.

Length (single mode)-km [Address A0h, Byte 14]

Addition to EEPROM data from original GBIC definition. This value specifies the link length that is supported by the transceiver while operating in compliance with the applicable standards using single mode fiber. The value is in units of kilometers. A value of 255 means that the transceiver supports a link length greater than 254 km. A value of zero means that the transceiver does not support single mode fiber or that the length information must be determined from the transceiver technology.

Length (single mode)-(100's)m [Address A0h, Byte 15]

This value specifies the link length that is supported by the transceiver while operating in compliance with the applicable standards using single mode fiber. The value is in units of 100 meters. A value of 255 means that the transceiver supports a link length greater than 25.4 km. A value of zero means that the transceiver does not support single mode fiber or that the length information must be determined from the transceiver technology.

Length (50um, OM2) [Address A0h, Byte 16]

This value specifies link length that is supported by the transceiver while operating in compliance with applicable standards using 50 micron multimode OM2 [500MHz*km at 850nm,] fiber. The value is in units of 10 meters. A value of 255 means that the transceiver supports a link length greater than 2.54 km. A value of zero means that the transceiver does not support 50 micron multimode fiber or that the length information must be determined from the transceiver technology.

Length (62.5um, OM1) [Address A0h, Byte 17]

This value specifies link length that is supported by the transceiver while operating in compliance with applicable standards using 62.5 micron multimode OM1 [200 MHz*km at 850nm, 500 MHz*km at 1310nm] fiber. The value is in units of 10 meters. A value of 255 means that the transceiver supports a link length greater than 2.54 km. A value of zero means that the transceiver does not support 62.5 micron multimode fiber or that the length information must determined from the transceiver technology. It is common for a multimode transceiver to support OM1, OM2 and OM3 fiber.

Length (Active Cable or Copper) [Address A0h, Byte 18]

This value specifies minimum link length supported by the transceiver while operating in compliance with applicable standards using copper cable. For active cable, this value represents actual length. The value is in units of 1 meter. A value of 255 means the transceiver supports a link length greater than 254 meters. A value of zero means the transceiver does not support copper or active cables or the length information must be determined from transceiver technology. Further information about cable design, equalization, and connectors is usually required to guarantee meeting a particular length requirement.

Length (50um, OM3) [Address A0h, Byte 19]

This value specifies link length that is supported by the transceiver while operating in compliance with applicable standards using 50 micron multimode OM3 [2000 MHz*km] fiber. The value is in units of 10 meters. A value of 255 means that the transceiver supports a link length greater than 2.54 km. A value of zero means that the transceiver does not support 50 micron multimode fiber or that the length information must be determined from the transceiver technology.

Vendor name [Address A0h, Bytes 20-35]

The vendor name is a 16 character field that contains ASCII characters, left-aligned and padded on the right with ASCII spaces (20h). The vendor name shall be the full name of the corporation, a commonly accepted abbreviation of the name of the corporation, the SCSI company code for the corporation, or the stock exchange code for the corporation. At least one of the vendor name or the vendor OUI fields shall contain valid data.

Vendor OUI [Address A0h, Bytes 37-39]

The vendor organizationally unique identifier field (vendor OUI) is a 3-byte field that contains the IEEE Company Identifier for the vendor. A value of all zero in the 3-byte field indicates that the Vendor OUI is unspecified.

Vendor PN [Address A0h, Bytes 40-55]

The vendor part number (vendor PN) is a 16-byte field that contains ASCII characters, left-aligned and padded on the right with ASCII spaces (20h), defining the vendor part number or product name. A value of all zero in the 16-byte field indicates that the vendor PN is unspecified.

Vendor Rev [Address A0h, Bytes 56-59]

The vendor revision number (vendor rev) is a 4-byte field that contains ASCII characters, left-aligned and padded on the right with ASCII spaces (20h), defining the vendor's product revision number. A value of all zero in the 4-byte field indicates that the vendor revision is unspecified.

Laser Wavelength (optical variants) & Cable Specification Compliance (passive or active cable variants) [Address A0h, Bytes 60-61]

For optical variants, as defined by having zero's in A0h Byte 8 bits 2 and 3, Bytes 60 and 61 denote nominal transmitter output wavelength at room temperature. 16 bit value with byte 60 as high order byte and byte 61 as low order byte. The laser wavelength is equal to the the 16 bit integer value in nm. This field allows the user to read the laser wavelength directly, so it is not necessary to infer it from the transceiver "Code for Electronic Compatibility" (bytes 3 to 10). This also allows specification of wavelengths not covered in bytes 3 to 10, such as those used in coarse WDM systems.

For passive/active cable variants, as defined in byte 8 (bits 2 or 3), see Tables 3.6b and 3.6c below for cable specification compliance details.

A value of 00h for both A0h Byte 60 and Byte 61 denotes laser wavelength or cable specification compliance is unspecified.

Table 3.6b: Passive Cable Specification Compliance (A0h Byte 8 Bit 2 set)

Data Addr	Bit	Description of cable	Data Addr	Bit	Description of cable
60	7	Unallocated	61	7	Unallocated
60	6	Unallocated	61	6	Unallocated
60	5	Reserved for SFF-8461	61	5	Unallocated
60	4	Reserved for SFF-8461	61	4	Unallocated
60	3	Reserved for SFF-8461	61	3	Unallocated
60	2	Reserved for SFF-8461	61	2	Unallocated
60	1	Compliant to FC-PI-4 Appendix H	61	1	Unallocated
60	0	Compliant to SFF-8431 Appendix E	61	0	Unallocated

Table 3.6c: Active Cable Specification Compliance (A0h Byte 8 Bit 3 set)

Data Addr	Bit	Description of cable	Data Addr	Bit	Description of cable
60	7	Unallocated	61	7	Unallocated
60	6	Unallocated	61	6	Unallocated
60	5	Unallocated	61	5	Unallocated
60	4	Unallocated	61	4	Unallocated
60	3	Compliant to FC-PI-4 Limiting	61	3	Unallocated
60	2	Compliant to SFF-8431 Limiting	61	2	Unallocated
60	1	Compliant to FC-PI-4 Appendix H	61	1	Unallocated
60	0	Compliant to SFF-8431 Appendix E	61	0	Unallocated

CC_BASE [Address A0h, Byte 63]

The check code is a one byte code that can be used to verify that the first 64 bytes of two-wire interface information in the SFP is valid. The check code shall be the low order 8 bits of the sum of the contents of all the bytes from byte 0 to byte 62, inclusive.

Options [Address A0h, Bytes 64-65]

The bits in the option field shall specify the options implemented in the transceiver as described in Table 3.7.

Table 3.7: Option values

A0h data address	bit	Description of option
64	7-3	Unallocated
	2	Cooled Transceiver Declaration (see SFF-8431). Value of zero identifies a conventional uncooled (or unspecified) laser implementation. Value of one identifies a cooled laser transmitter implementation.
	1	Power Level Declaration (see SFF-8431). Value of zero identifies Power Level 1 (or unspecified) requirements. Value of one identifies Power Level 2 requirement. See Table 3.11 and Table 3.18a for control, status, timing.
	0	Linear Receiver Output Implemented (see SFF-8431). Value of zero identifies a conventional limiting (or unspecified) receiver output. Value of one identifies a linear receiver output.
65	7-6	Unallocated
	5	RATE_SELECT functionality is implemented NOTE: Lack of implemention does not indicate lack of simultaneous compliance with multiple standard rates. Compliance with particular standards should be determined from Transceiver Code Section (Table 3.5). Refer to Table 3.6a for Rate_Select functionality type identifiers.
	4	TX_DISABLE is implemented and disables the high speed serial output.
	3	TX_FAULT signal implemented. (See SFP MSA)
	2	Loss of Signal implemented, signal inverted from standard definition in SFP MSA (often called "Signal Detect"). NOTE: This is not standard SFP/GBIC behavior and should be avoided, since non-interoperable behavior results.
	1	Loss of Signal implemented, signal as defined in SFP MSA (often called "Rx_LOS").
	0	Unallocated

BR, max [Address A0h, Byte 66]

The upper bit rate limit at which the transceiver will still meet its specifications (BR, max) is specified in units of 1% above the nominal bit rate. A value of zero indicates that this field is not specified.

BR, min [Address A0h, Byte 67]

The lower bit rate limit at which the transceiver will still meet its specifications (BR, min) is specified in units of 1% below the nominal bit rate. A value of zero indicates that this field is not specified.

Vendor SN [Address A0h, Bytes 68-83]

The vendor serial number (vendor SN) is a 16 character field that contains ASCII characters, left-aligned and padded on the right with ASCII spaces (20h), defining the vendor's serial number for the transceiver. A value of all zero in the 16-byte field indicates that the vendor SN is unspecified.

Date Code [Address A0h, Bytes 84-91]

The date code is an 8-byte field that contains the vendor's date code in ASCII characters. The date code is mandatory. The date code shall be in the format specified by Table 3.8.

Table 3.8: Date Code

A0h Data Address	Description of field
84-85	ASCII code, two low order digits of year. (00 = 2000).
86-87	ASCII code, digits of month (01 = Jan through 12 = Dec)
88-89	ASCII code, day of month (01 - 31)
90-91	ASCII code, vendor specific lot code, may be blank

Diagnostic Monitoring Type [Address A0h, Byte 92]

"Diagnostic Monitoring Type" is a 1 byte field with 8 single bit indicators describing how diagnostic monitoring is implemented in the particular transceiver.

Note that if bit 6, address 92 is set indicating that digital diagnostic monitoring has been implemented, received power monitoring, transmitted power monitoring, bias current monitoring, supply voltage monitoring and temperature monitoring must all be implemented. Additionally, alarm and warning thresholds must be written as specified in this document at locations 00 to 55 on 2 wire serial address 1010001X (A2h) (see Table 3.9).

Two calibration options are possible if bit 6 has been set indicating that digital diagnostic monitoring has been implemented. If bit 5, "Internally calibrated", is set, the transceiver directly reports calibrated values in units of current, power etc. If bit 4, "Externally calibrated", is set, the reported values are A/D counts which must be converted to real world units using calibration values read using 2 wire serial address 1010001X (A2h) from bytes 56 to 95. See "Diagnostics" section for details.

Bit 3 indicates whether the received power measurement represents average input optical power or OMA. If the bit is set, average power is monitored. If it is not, OMA is monitored.

Addressing Modes

Bit 2 indicates whether or not it is necessary for the host to perform an address change sequence before accessing information at 2-wire serial address A2h. If this bit is not set, the host may simply read from either address, A0h or A2h, by using that value in the address byte during the 2-wire communication sequence. If the bit is set, the following sequence must be executed prior to accessing information at address A2h. Once A2h has been accessed, it will be necessary to execute the address change sequence again prior to reading from A0h. The address change sequence is defined as the following steps on the 2 wire serial interface:

1) Host controller performs a Start condition, followed by a slave address of 0b00000000.
   Note that the R/W bit of this address indicates transfer from host to device (‘0’b).
2) Device responds with Ack
3) Host controller transfers 0b00000100 (04h) as the next 8 bits of data
   This value indicates that the device is to change its address
4) Device responds with Ack
5) Host controller transfers one of the following values as the next 8 bits of data:
   0bXXXXXX00 – specifies Two-wire interface ID memory page
   0bXXXXXX10 – specifies Digital Diagnostic memory page
6) Device responds with Ack
7) Host controller performs a Stop condition
8) Device changes address that it responds to, based on the Step 5 byte value above:
   0bXXXXXX00 – address becomes 0b1010000X (A0h)
   0bXXXXXX10 – address becomes 0b1010001X (A2h)

Table 3.9: Diagnostic Monitoring Type

A0h Data Address	Bit	Description
92	7	Reserved for legacy diagnostic implementations. Must be ‘0’ for compliance with this document.
	6	Digital diagnostic monitoring implemented (described in this document). Must be ‘1’ for compliance with this document.
	5	Internally calibrated
	4	Externally calibrated
	3	Received power measurement type 0 = OMA, 1 = average power
	2	Address change required see section above, “addressing modes”
	1-0	Unallocated

Enhanced Options [Address A0h, Byte 93]

“Enhanced Options” is a one byte field with 8 single bit indicators which describe the optional digital diagnostic features implemented in the transceiver. Since transceivers will not necessarily implement all optional features described in this document, the “Enhanced Options” bit field allows the host system to determine which functions are available over the 2 wire serial bus. A ‘1’ indicates that the particular function is implemented in the transceiver. Bits 3 and 6 of byte 110 (see Table 3.17) allow the user to control the Rate_Select and TX_Disable functions. If these functions are not implemented, the bits remain readable and writable, but the transceiver ignores them.

Note that “soft” functions of TX_DISABLE, TX_FAULT, RX_LOS, and RATE_SELECT do not meet timing requirements as specified in the SFP MSA section B3 “Timing Requirements of Control and Status I/O” and the GBIC Specification, revision 5.5, (SFF-8053), section 5.3.1, for their corresponding pins. The soft functions allow a host to poll or set these values over the two-wire interface bus as an alternative to monitoring/setting pin values. Timing is vendor specific, but must meet the requirements specified in Table 3.11 below. Asserting either the “hard pin” or “soft bit” (or both) for TX_DISABLE or RATE_SELECT will result in that function being asserted.

Table 3.10: Enhanced Options

A0h Address	Bit	Description
93	7	Optional Alarm/warning flags implemented for all monitored quantities (see Table 3.18)
	6	Optional soft TX_DISABLE control and monitoring implemented
	5	Optional soft TX_FAULT monitoring implemented
	4	Optional soft RX_LOS monitoring implemented
	3	Optional soft RATE_SELECT control and monitoring implemented
	2	Optional Application Select control implemented per SFF-8079
	1	Optional soft Rate Select control implemented per SFF-8431
	0	Unallocated

Table 3.11: I/O Timing for Soft (via 2-wire interface) Control & Status Functions

Parameter	Symbol	Min	Max	Units	Conditions
TX_DISABLE assert time	t_off		100	ms	Time from TX_DISABLE bit set[1] until optical output falls below 10% of nominal
TX_DISABLE deassert time	t_on		100	ms	Time from TX_DISABLE bit cleared[1] until optical output rises above 90% of nominal
Time to initialize, including reset of TX_FAULT	t_init		300	ms	Time from power on or negation of TX_FAULT using TX_DISABLE until transmitter output is stable[2].
TX_FAULT assert time	t_fault		100	ms	Time from fault to TX_FAULT bit set.
RX_LOS assert time	t_loss_on		100	ms	Time from LOS state to RX_LOS bit set
RX_LOS deassert time	t_loss_off		100	ms	Time from non-LOS state to RX_LOS bit cleared
Rate select change time	t_rate_select		100 [3]	ms	Time from change of state of Rate Select bit[1] until receiver bandwidth is in conformance with appropriate specification
Two-wire serial interface Clock rate	f_serial_clock		100	kHz	n/a
Two-wire serial interface Diagnostic data ready time	t_data		1000	ms	From power on to data ready, bit 0 of byte 110 set
Two-wire serial interface Bus hardware ready time	t_serial		300	ms	Time from power on until module is ready for data transmission over the two wire serial bus.
Optional. Power Level 2 assert time (per SFF-8431)	t_power_level2		300	ms	Time from Power Level 2 enable bit set until module operation is stable. See Table 3.18a for control bit.

[1] Measured from falling clock edge after stop bit of write transaction.
[2] See Gigabit Interface Converter (GBIC). SFF-8053, rev. 5.5, September 27, 2000
[3.] The T11.2 committee, as part of its FC-PI-2 standardization effort, has advised that a 1ms maximum is required to be compatible with auto-negotiation algorithms documented in the FC-FS specification.

SFF-8472 Compliance [Address A0h, Byte 94]

Byte 94 contains an unsigned integer that indicates which feature set(s) are implemented in the transceiver.

Table 3.12: SFF-8472 Compliance

A0h Data Address	Value	Interpretation
94	00h	Digital diagnostic functionality not included or undefined.
	01h	Includes functionality described in Rev 9.3 of SFF-8472.
	02h	Includes functionality described in Rev 9.5 of SFF-8472.
	03h	Includes functionality described in Rev 10.2 of SFF-8472.
	04h	Includes functionality described in Rev 10.4 of SFF-8472.
	05h	Includes functionality described in Rev 10.5 of SFF-8472.
	06h – FFh	Unallocated

CC_EXT [Address A0h, Byte 95]

The check code is a one byte code that can be used to verify that the first 32 bytes of extended two-wire interface information in the SFP is valid. The check code shall be the low order 8 bits of the sum of the contents of all the bytes from byte 64 to byte 94, inclusive.

Diagnostics Overview [Address A2h]

2 wire serial bus address 1010001X (A2h) is used to access measurements of transceiver temperature, internally measured supply voltage, TX bias current, TX output power, received optical power, and two additional quantities to be defined in the future.

The values are interpreted differently depending upon the option bits set at address 92. If bit 5 “internally calibrated” is set, the values are calibrated absolute measurements, which should be interpreted according to the section “Internal Calibration” below. If bit 4 “externally calibrated” is set, the values are A/D counts, which are converted into real units per the subsequent section titled “External Calibration”.

Measured parameters are reported in 16 bit data fields, i.e., two concatenated bytes. The 16 bit data fields allow for wide dynamic range. This is not intended to imply that a 16 bit A/D system is recommended or required in order to achieve the accuracy goals stated below. The width of the data field should not be taken to imply a given level of precision. It is conceivable that the accuracy goals herein can be achieved by a system having less than 16 bits of resolution. It is recommended that any low-order data bits beyond the system’s specified accuracy be fixed at zero. Overall system accuracy and precision will be vendor dependent.

To guarantee coherency of the diagnostic monitoring data, the host is required to retrieve any multi-byte fields from the diagnostic monitoring data structure (IE: Rx Power MSB - byte 104 in A2h, Rx Power LSB - byte 105 in A2h) by the use of a single two-byte read sequence across the two-wire interface interface.

The transceiver is required to ensure that any multi-byte fields which are updated with diagnostic monitoring data (e.g. Rx Power MSB - byte 104 in A2h, Rx Power LSB - byte 105 in A2h) must have this update done in a fashion which guarantees coherency and consistency of the data. In other words, the update of a multi-byte field by the transceiver must not occur such that a partially updated multi-byte field can be transferred to the host. Also, the transceiver shall not update a multi-byte field within the structure during the transfer of that multi-byte field to the host, such that partially updated data would be transferred to the host.

Accuracy requirements specified below shall apply to the operating signal range specified in the relevant standard. The manufacturer’s specification should be consulted for more detail on the conditions under which the accuracy requirements are met.

Internal Calibration

Measurements are calibrated over vendor specified operating temperature and voltage and should be interpreted as defined below. Alarm and warning threshold values should be interpreted in the same manner as real time 16 bit data.

1) Internally measured transceiver temperature. Represented as a 16 bit signed twos complement value in increments of 1/256 degrees Celsius, yielding a total range of -128C to +128C. Temperature accuracy is vendor specific but must be better than ±3 degrees Celsius over specified operating temperature and voltage. Please see vendor specification for details on location of temperature sensor. The temperature in degrees Celsius is given by the signed twos complement value with LSB equal to 1/256 C. See Tables 3.13 and 3.14 below for examples of temperature format.

2) Internally measured transceiver supply voltage. Represented as a 16 bit unsigned integer with the voltage defined as the full 16 bit value (0 – 65535) with LSB equal to 100 uVolt, yielding a total range of 0 to +6.55 Volts. Practical considerations to be defined by transceiver manufacturer will tend to limit the actual bounds of the supply voltage measurement. Accuracy is vendor specific but must be better than ±3% of the manufacturer's nominal value over specified operating temperature and voltage. Note that in some transceivers, transmitter supply voltage and receiver supply voltage are isolated. In that case, only one supply is monitored. Refer to the device specification for more detail.

3) Measured TX bias current in uA. Represented as a 16 bit unsigned integer with the current defined as the full 16 bit value (0 – 65535) with LSB equal to 2 uA, yielding a total range of 0 to 131 mA. Accuracy is vendor specific but must be better than ±10% of the manufacturer's nominal value over specified operating temperature and voltage.

4) Measured TX output power in mW. Represented as a 16 bit unsigned integer with the power defined as the full 16 bit value (0 – 65535) with LSB equal to 0.1 uW, yielding a total range of 0 to 6.5535 mW (~ -40 to +8.2 dBm). Data is assumed to be based on measurement of laser monitor photodiode current. It is factory calibrated to absolute units using the most representative fiber output type. Accuracy is vendor specific but must be better than ±3dB over specified temperature and voltage. Data is not valid when the transmitter is disabled.

5) Measured RX received optical power in mW. Value can represent either average received power or OMA depending upon how bit 3 of byte 92 (A0h) is set. Represented as a 16 bit unsigned integer with the power defined as the full 16 bit value (0 – 65535) with LSB equal to 0.1 uW, yielding a total range of 0 to 6.5535 mW (~ -40 to +8.2 dBm). Absolute accuracy is dependent upon the exact optical wavelength. For the vendor specified wavelength, accuracy shall be better than ±3dB over specified temperature and voltage. This accuracy shall be maintained for input power levels up to the lesser of maximum transmitted or maximum received optical power per the appropriate standard. It shall be maintained down to the minimum transmitted power minus cable plant loss (insertion loss or passive loss) per the appropriate standard. Absolute accuracy beyond this minimum required received input optical power range is vendor specific.

Tables 3.13 and 3.14 below illustrate the 16 bit signed twos complement format used for temperature reporting. The most significant bit (D7) represents the sign, which is zero for positive temperatures and one for negative temperatures.

Table 3.13: Bit weights (°C) for temperature reporting registers

Most Significant Byte (byte 96)								Least Significant Byte (byte 97)							
D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
SIGN	64	32	16	8	4	2	1	1/2	1/4	1/8	1/16	1/32	1/64	1/128	1/256

Table 3.14: Digital temperature format

Temperature		BINARY		HEXADECIMAL	
DECIMAL	FRACTION	HIGH BYTE	LOW BYTE	HIGH BYTE	LOW BYTE
+127.996	+127 255/256	01111111	11111111	7F	FF
+125.000	+125	01111101	00000000	7D	00
+25.000	+25	00011001	00000000	19	00
+1.004	+1 1/256	00000001	00000001	01	01
+1.000	+1	00000001	00000000	01	00
+0.996	+255/256	00000000	11111111	00	FF
+0.004	+1/256	00000000	00000001	00	01
0.000	0	00000000	00000000	00	00
-0.004	-1/256	11111111	11111111	FF	FF
-1.000	-1	11111111	00000000	FF	00
-25.000	-25	11100111	00000000	E7	00
-40.000	-40	11011000	00000000	D8	00
-127.996	-127 255/256	10000000	00000001	80	01
-128.000	-128	10000000	00000000	80	00

External Calibration

Measurements are raw A/D values and must be converted to real world units using calibration constants stored in EEPROM locations 56 – 95 at 2 wire serial bus address A2h. Calibration is valid over vendor specified operating temperature and voltage. Alarm and warning threshold values should be interpreted in the same manner as real time 16 bit data.

After calibration per the equations given below for each variable, the results are consistent with the accuracy and resolution goals for internally calibrated devices.

1) Internally measured transceiver temperature. Module temperature, T, is given by the following equation: $T(C) = T_{slope} * T_{AD}$ (16 bit signed twos complement value) + T_{offset}. The result is in units of 1/256C, yielding a total range of –128C to +128C. See Table 3.16 for locations of T_{SLOPE} and T_{OFFSET}. Temperature accuracy is vendor specific but must be better than ±3 degrees Celsius over specified operating temperature and voltage. Please see vendor specification sheet for details on location of temperature sensor. Tables 3.13 and 3.14 above give examples of the 16 bit signed twos complement temperature format.

2) Internally measured supply voltage. Module internal supply voltage, V, is given in microvolts by the following equation: $V(uV) = V_{SLOPE} * V_{AD}$ (16 bit unsigned integer) + V_{OFFSET}. The result is in units of 100uV, yielding a total range of 0 – 6.55V. See Table 3.16 for locations of V_{SLOPE} and V_{OFFSET}. Accuracy is vendor specific but must be better than ±3% of the manufacturer's nominal value over specified operating temperature and voltage. Note that in some transceivers, transmitter supply voltage and receiver supply voltage are isolated. In that case, only one supply is monitored. Refer to the manufacturer's specification for more detail.

3) Measured transmitter laser bias current. Module laser bias current, I, is given in microamps by the following equation: $I (uA) = I_{SLOPE} * I_{AD}$ (16 bit unsigned integer) + I_{OFFSET}. This result is in units of 2 uA, yielding a total range of 0 to 131 mA. See Table 3.16 for locations of I_{SLOPE} and I_{OFFSET}. Accuracy is vendor specific but must be better than ±10% of the manufacturer's nominal value over specified operating temperature and voltage.

4) Measured coupled TX output power. Module transmitter coupled output power, TX_PWR, is given in uW by the following equation: $TX\_PWR (uW) = TX\_PWR_{SLOPE} * TX\_PWR_{AD}$ (16 bit unsigned integer) + TX_PWR_{OFFSET}. This result is in units of 0.1uW yielding a total range of 0 – 6.5mW. See Table 3.16 for locations of TX_PWR_{SLOPE} and TX_PWR_{OFFSET}. Accuracy is vendor specific but must be better than ±3dB over specified operating temperature and voltage. Data is assumed to be based on measurement of a laser monitor photodiode current. It is factory calibrated to absolute units using the most representative fiber output type. Data is not valid when the transmitter is disabled.

5) Measured received optical power. Received power, RX_PWR, is given in uW by the following equation:

$$
\begin{aligned}
\text{Rx\_PWR (uW)} = \; & \text{Rx\_PWR(4)} * \text{Rx\_PWR}_{AD}{}^{4} \text{ (16 bit unsigned integer)} + \\
& \text{Rx\_PWR(3)} * \text{Rx\_PWR}_{AD}{}^{3} \text{ (16 bit unsigned integer)} + \\
& \text{Rx\_PWR(2)} * \text{Rx\_PWR}_{AD}{}^{2} \text{ (16 bit unsigned integer)} + \\
& \text{Rx\_PWR(1)} * \text{Rx\_PWR}_{AD} \text{ (16 bit unsigned integer)} + \\
& \text{Rx\_PWR(0)}
\end{aligned}
$$

The result is in units of 0.1uW yielding a total range of 0 – 6.5mW. See Table 3.16 for locations of Rx_PWR(4-0). Absolute accuracy is dependent upon the exact optical wavelength. For the vendor specified wavelength, accuracy shall be better than ±3dB over specified temperature and voltage. This accuracy shall be maintained for input power levels up to the lesser of maximum transmitted or maximum received optical power per the appropriate standard. It shall be maintained down to the minimum transmitted power minus cable plant loss (insertion loss or passive loss) per the appropriate standard. Absolute accuracy beyond this minimum required received input optical power range is vendor specific.

Alarm and Warning Thresholds [Address A2h, Bytes 0-39]

Each A/D quantity has a corresponding high alarm, low alarm, high warning and low warning threshold. These factory preset values allow the user to determine when a particular value is outside of "normal" limits as determined by the transceiver manufacturer. It is assumed that these values will vary with different technologies and different implementations. When external calibration is used, data may be compared to alarm and warning threshold values before or after calibration by the host. Comparison can be done directly before calibration. If comparison is to be done after calibration, calibration must first be applied to both data and threshold values.

The values reported in the alarm and warning thresholds area (see below) may be temperature compensated or otherwise adjusted when setting warning and/or alarm flags. Any threshold compensation or adjustment is vendor specific and optional. See vendor's data sheet for use of alarm and warning thresholds.

Table 3.15: Alarm and Warning Thresholds (2-Wire Address A2h)

Address	# Bytes	Name	Description
00-01	2	Temp High Alarm	MSB at low address
02-03	2	Temp Low Alarm	MSB at low address
04-05	2	Temp High Warning	MSB at low address
06-07	2	Temp Low Warning	MSB at low address
08-09	2	Voltage High Alarm	MSB at low address
10-11	2	Voltage Low Alarm	MSB at low address
12-13	2	Voltage High Warning	MSB at low address
14-15	2	Voltage Low Warning	MSB at low address
16-17	2	Bias High Alarm	MSB at low address
18-19	2	Bias Low Alarm	MSB at low address
20-21	2	Bias High Warning	MSB at low address
22-23	2	Bias Low Warning	MSB at low address
24-25	2	TX Power High Alarm	MSB at low address
26-27	2	TX Power Low Alarm	MSB at low address
28-29	2	TX Power High Warning	MSB at low address
30-31	2	TX Power Low Warning	MSB at low address
32-33	2	RX Power High Alarm	MSB at low address
34-35	2	RX Power Low Alarm	MSB at low address
36-37	2	RX Power High Warning	MSB at low address
38-39	2	RX Power Low Warning	MSB at low address
40-55	16	Unallocated	Reserved for future monitored quantities

Calibration Constants [Address A2h, Bytes 56-91]

TABLE 3.16: Calibration constants for External Calibration Option (2 Wire Address A2h)

Address	# Bytes	Name	Description
56-59	4	Rx_PWR(4)	Single precision floating point calibration data - Rx optical power. Bit 7 of byte 56 is MSB. Bit 0 of byte 59 is LSB. Rx_PWR(4) should be set to zero for “internally calibrated” devices.
60-63	4	Rx_PWR(3)	Single precision floating point calibration data - Rx optical power. Bit 7 of byte 60 is MSB. Bit 0 of byte 63 is LSB. Rx_PWR(3) should be set to zero for “internally calibrated” devices.
64-67	4	Rx_PWR(2)	Single precision floating point calibration data, Rx optical power. Bit 7 of byte 64 is MSB, bit 0 of byte 67 is LSB. Rx_PWR(2) should be set to zero for “internally calibrated” devices.
68-71	4	Rx_PWR(1)	Single precision floating point calibration data, Rx optical power. Bit 7 of byte 68 is MSB, bit 0 of byte 71 is LSB. Rx_PWR(1) should be set to 1 for “internally calibrated” devices.
72-75	4	Rx_PWR(0)	Single precision floating point calibration data, Rx optical power. Bit 7 of byte 72 is MSB, bit 0 of byte 75 is LSB. Rx_PWR(0) should be set to zero for “internally calibrated” devices.
76-77	2	Tx_I(Slope)	Fixed decimal (unsigned) calibration data, laser bias current. Bit 7 of byte 76 is MSB, bit 0 of byte 77 is LSB. Tx_I(Slope) should be set to 1 for “internally calibrated” devices.
78-79	2	Tx_I(Offset)	Fixed decimal (signed two’s complement) calibration data, laser bias current. Bit 7 of byte 78 is MSB, bit 0 of byte 79 is LSB. Tx_I(Offset) should be set to zero for “internally calibrated” devices.
80-81	2	Tx_PWR(Slope)	Fixed decimal (unsigned) calibration data, transmitter coupled output power. Bit 7 of byte 80 is MSB, bit 0 of byte 81 is LSB. Tx_PWR(Slope) should be set to 1 for “internally calibrated” devices.
82-83	2	Tx_PWR(Offset)	Fixed decimal (signed two’s complement) calibration data, transmitter coupled output power. Bit 7 of byte 82 is MSB, bit 0 of byte 83 is LSB. Tx_PWR(Offset) should be set to zero for “internally calibrated” devices.
84-85	2	T (Slope)	Fixed decimal (unsigned) calibration data, internal module temperature. Bit 7 of byte 84 is MSB, bit 0 of byte 85 is LSB. T(Slope) should be set to 1 for “internally calibrated” devices.
86-87	2	T (Offset)	Fixed decimal (signed two’s complement) calibration data, internal module temperature. Bit 7 of byte 86 is MSB, bit 0 of byte 87 is LSB. T(Offset) should be set to zero for “internally calibrated” devices.
88-89	2	V (Slope)	Fixed decimal (unsigned) calibration data, internal module supply voltage. Bit 7 of byte 88 is MSB, bit 0 of byte 89 is LSB. V(Slope) should be set to 1 for “internally calibrated” devices.
90-91	2	V (Offset)	Fixed decimal (signed two’s complement) calibration data, internal module supply voltage. Bit 7 of byte 90 is MSB. Bit 0 of byte 91 is LSB. V(Offset) should be set to zero for “internally calibrated” devices.
92-94	3	Unallocated	
95	1	Checksum	Byte 95 contains the low order 8 bits of the sum of bytes 0 – 94.

The slope constants at addresses 76, 80,84, and 88, are unsigned fixed-point binary numbers. The slope will therefore always be positive. The binary point is in between the upper and lower bytes, i.e., between the eight and ninth most significant bits. The most significant byte is the integer portion in the range 0 to +255. The least significant byte represents the fractional portion in the range of 0.00391 (1/256) to 0.9961 (255/256). The smallest real number that can be represented by this format is 0.00391 (1/256); the largest real number that can be represented using this format is 255.9961 (255 + 255/256). Slopes are defined, and conversion formulas found, in the "External Calibration" section. Examples of this format are illustrated below:

Table 3.16a: Unsigned fixed-point binary format for slopes

Decimal Value	Binary Value		Hexadecimal Value	
	MSB	LSB	High Byte	Low Byte
0.0000	00000000	00000000	00	00
0.0039	00000000	00000001	00	01
1.0000	00000001	00000000	01	00
1.0313	00000001	00001000	01	08
1.9961	00000001	11111111	01	FF
2.0000	00000010	00000000	02	00
255.9921	11111111	11111110	FF	FE
255.9961	11111111	11111111	FF	FF

The calibration offsets are 16-bit signed twos complement binary numbers. The offsets are defined by the formulas in the "External Calibration" section. The least significant bit represents the same units as described above under "Internal Calibration" for the corresponding analog parameter, e.g., 2µA for bias current, 0.1µW for optical power, etc. The range of possible integer values is from +32767 to -32768. Examples of this format are shown below.

Table 3.16b: Format for offsets

Decimal Value	Binary Value		Hexadecimal Value	
	High Byte	Low Byte	High Byte	Low Byte
+32767	01111111	1111111	7F	FF
+3	00000000	00000011	00	03
+2	00000000	00000010	00	02
+1	00000000	00000001	00	01
0	00000000	00000000	00	00
-1	11111111	11111111	FF	FF
-2	11111111	11111110	FF	FE
-3	11111111	11111101	FF	FD
-32768	10000000	00000000	80	00

External calibration of received optical power makes use of single-precision floating-point numbers as defined by *IEEE Standard for Binary Floating-Point Arithmetic*, IEEE Std 754-1985. Briefly, this format utilizes four bytes (32 bits) to represent real numbers. The first and most significant bit is the sign bit; the next eight bits indicate an exponent in the range of +126 to –127; the remaining 23 bits represent the mantissa. The 32 bits are therefore arranged as in Table 3.16c below.

Table 3.16c: IEEE-754 Single-Precision Floating Point Number Format

<table>
<tr><td>FUNCTION</td><td>SIGN</td><td>EXPONENT</td><td colspan="4">MANTISSA</td></tr>
<tr><td>BIT</td><td>31</td><td>30…………………23</td><td colspan="4">22…………………………………………………………0</td></tr>
<tr><td>BYTE</td><td colspan="3">3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">← Most Significant</td><td colspan="3">Least Significant →</td></tr>
</table>

Rx_PWR(4), as an example, is stored as in Table 3.16d.

Table 3.16d: Example of Floating Point Representation

BYTE ADDRESS	CONTENTS	SIGNIFICANCE
56	SEEEEEEE	Most
57	EMMMMMMM	2nd Most
58	MMMMMMMM	2nd Least
59	MMMMMMMM	Least

where S = sign bit; E = exponent bit; M = mantissa bit.

Special cases of the various bit values are reserved to represent indeterminate values such as positive and negative infinity; zero; and “NaN” or not a number. NaN indicates an invalid result. As of this writing, explanations of the IEEE single precision floating point format were posted on the worldwide web at

http://www.psc.edu/general/software/packages/ieee/ieee.html

and

http://research.microsoft.com/~hollasch/cgindex/coding/ieeefloat.html.

The actual IEEE standard is available at www.IEEE.org

CC_DMI [Address A2h, Byte 95]

This check sum is a one byte code that can be used to verify that the first 94 bytes of factory programmed “diagnostic management interface” information in the SFP is valid. The check code shall be the low order 8 bits of the sum of the contents of all the bytes from byte 0 to byte 94, inclusive.

.

Real Time Diagnostic and Control Registers [Address A2h, Bytes 96-111]

TABLE 3.17: A/D Values and Status Bits (2 Wire Address A2h)

Byte	Bit	Name	Description
Converted analog values. Calibrated 16 bit data.			
96	All	Temperature MSB	Internally measured module temperature.
97	All	Temperature LSB	
98	All	Vcc MSB	Internally measured supply voltage in transceiver.
99	All	Vcc LSB	
100	All	TX Bias MSB	Internally measured TX Bias Current.
101	All	TX Bias LSB	
102	All	TX Power MSB	Measured TX output power.
103	All	TX Power LSB	
104	All	RX Power MSB	Measured RX input power.
105	All	RX Power LSB	
106-109	All	Unallocated	Reserved for future diagnostic definitions
Optional Status/Control Bits			
110	7	TX Disable State	Digital state of the TX Disable Input Pin. Updated within 100ms of change on pin.
	6	Soft TX Disable Select	Read/write bit that allows software disable of laser. Writing ‘1’ disables laser. See Table 3.11 for enable/disable timing requirements. This bit is “OR”d with the hard TX_DISABLE pin value. Note, per SFP MSA TX_DISABLE pin is default enabled unless pulled low by hardware. If Soft TX Disable is not implemented, the transceiver ignores the value of this bit. Default power up value is zero/low.
	5	RS(1) State	Digital state of SFP input pin AS(1) per SFF-8079 or RS(1) per SFF-8431. Updated within 100ms of change on pin. See A2h Byte 118, Bit 3 for Soft RS(1) Select control information.
	4	Rate_Select State [aka. “RS(0)”]	Digital state of the SFP Rate_Select Input Pin. Updated within 100ms of change on pin. Note: This pin is also known as AS(0) in SFF-8079 and RS(0) in SFF-8431.
	3	Soft Rate_Select Select [aka. “RS(0)”]	Read/write bit that allows software rate select control. Writing ‘1’ selects full bandwidth operation. This bit is “OR’d with the hard Rate_Select, AS(0) or RS(0) pin value. See Table 3.11 for timing requirements. Default at power up is logic zero/low. If Soft Rate Select is not implemented, the transceiver ignores the value of this bit. Note: Specific transceiver behaviors of this bit are identified in Table 3.6a and referenced documents. See Table 3.18a, byte 118, bit 3 for Soft RS(1) Select.
	2	TX Fault State	Digital state of the TX Fault Output Pin. Updated within 100ms of change on pin.
	1	Rx_LOS State	Digital state of the RX_LOS Output Pin. Updated within 100ms of change on pin.
	0	Data_Ready_Bar State	Indicates transceiver has achieved power up and data is ready. Bit remains high until data is ready to be read at which time the device sets the bit low.
111	7-0	Reserved	Reserved for SFF-8079.

The data_ready_bar bit is high during module power up and prior to the first valid A/D reading. Once the first valid A/D reading occurs, the bit is set low until the device is powered down. The bit must be set low within 1 second of power up.

Alarm and Warning Flags [Address A2h, Bytes 112-117]

Bytes 112 – 117 contain an optional set of alarm and warning flags. The flags may be latched or non-latched. Implementation is vendor specific, and the vendor's specification sheet should be consulted for details. It is recommended that in either case, detection of an asserted flag bit should be verified by a second read of the flag at least 100ms later. For users who do not wish to set their own threshold values or read the values in locations 0 - 55, the flags alone can be monitored. Two flag types are defined.

1) Alarm flags associated with transceiver temperature, supply voltage, TX bias current, TX output power and received optical power as well as reserved locations for future flags. Alarm flags indicate conditions likely to be associated with an in-operational link and cause for immediate action.

2) Warning flags associated with transceiver temperature, supply voltage, TX bias current, TX output power and received optical power as well as reserved locations for future flags. Warning flags indicate conditions outside the normally guaranteed bounds but not necessarily causes of immediate link failures. Certain warning flags may also be defined by the manufacturer as end-of-life indicators (such as for higher than expected bias currents in a constant power control loop).

Alarm and Warning Flags [Address A2h, Bytes 112-117]

Table 3.18: Alarm and Warning Flag Bits (2-Wire Address A2h)

Byte	Bit	Name	Description
Reserved Optional Alarm and Warning Flag Bits (See Notes 3-6)			
112	7	Temp High Alarm	Set when internal temperature exceeds high alarm level.
	6	Temp Low Alarm	Set when internal temperature is below low alarm level.
	5	Vcc High Alarm	Set when internal supply voltage exceeds high alarm level.
	4	Vcc Low Alarm	Set when internal supply voltage is below low alarm level.
	3	TX Bias High Alarm	Set when TX Bias current exceeds high alarm level.
	2	TX Bias Low Alarm	Set when TX Bias current is below low alarm level.
	1	TX Power High Alarm	Set when TX output power exceeds high alarm level.
	0	TX Power Low Alarm	Set when TX output power is below low alarm level.
113	7	RX Power High Alarm	Set when Received Power exceeds high alarm level.
	6	RX Power Low Alarm	Set when Received Power is below low alarm level.
	5	Reserved Alarm	
	4	Reserved Alarm	
	3	Reserved Alarm	
	2	Reserved Alarm	
	1	Reserved Alarm	
	0	Reserved Alarm	
114	All	Unallocated	
115	All	Unallocated	
116	7	Temp High Warning	Set when internal temperature exceeds high warning level.
	6	Temp Low Warning	Set when internal temperature is below low warning level.
	5	Vcc High Warning	Set when internal supply voltage exceeds high warning level.
	4	Vcc Low Warning	Set when internal supply voltage is below low warning level.
	3	TX Bias High Warning	Set when TX Bias current exceeds high warning level.
	2	TX Bias Low Warning	Set when TX Bias current is below low warning level.
	1	TX Power High Warning	Set when TX output power exceeds high warning level.
	0	TX Power Low Warning	Set when TX output power is below low warning level.
117	7	RX Power High Warning	Set when Received Power exceeds high warning level.
	6	RX Power Low Warning	Set when Received Power is below low warning level.
	5	Reserved Warning	
	4	Reserved Warning	
	3	Reserved Warning	
	2	Reserved Warning	
	1	Reserved Warning	
	0	Reserved Warning	

Extended Module Control/Status Bytes [Address A2h, Bytes 118-119]

Addresses 118 – 119 are defined for extended module control and status functions. Depending on usage, the contents may be writable by the host. See Table 3.7 for power level declaration requirement in Address 64, byte 1.

Table 3.18a: Extended Control/Status Memory Addresses (2-Wire Address A2h)

Byte	Bit	Name	Description
118	4-7	Reserved	
	3	Soft RS(1) Select	Read/write bit that allows software Tx rate control. Writing '1' selects full speed Tx operation. This bit is "OR'd with the hard RS(1) pin value. See Table 3.11 for timing requirements. Default at power up is logic zero/low. If Soft RS(1) is not implemented, the transceiver ignores the value of this bit. Note: Specific transceiver behaviors of this bit are identified in Table 3.6a and referenced documents. See Table 3.17, byte 110, bit 3 for Soft RS(0) Select.
	2	Reserved	
	1	Power Level Operation State	Optional. SFF-8431 Power Level (maximum power dissipation) status. Value of zero indicates Power Level 1 operation (1.0 Watt max). Value of one indicates Power Level 2 operation (1.5 Watt max). Refer to Table 3.7 for Power Level requirement declaration. Refer to Table 3.11 for timing.
	0	Power Level Select	Optional. SFF-8431 Power Level (maximum power dissipation) control bit. Value of zero enables Power Level 1 only (1.0 Watt max). Value of one enables Power Level 2 (1.5 Watt max). Refer to Table 3.7 for Power Level requirement declaration. Refer to Table 3.11 for timing. If Power Level 2 is not implemented, the SFP ignores the value of this bit.
119	7-0	Unallocated	

Vendor Specific Locations [Address A2h, Bytes 120-127]

Addresses 120 – 127 are defined for vendor specific memory functions. Potential usage includes vendor password field for protected functions, scratch space for calculations or other proprietary content.

Table 3.19: Vendor Specific Memory Addresses (2-Wire Address A2h)

Address	# Bytes	Name	Description
120-127	8	Vendor Specific	Vendor specific memory addresses

User Accessible EEPROM Locations [Address A2h, Bytes 128-247]

Addresses 128-247 represent 120 bytes of user/host writable non-volatile memory – for any reasonable use. Consult vendor datasheets for any limits on writing to these locations, including timing and maximum number of writes. Potential usage includes customer specific identification information, usage history statistics, scratch space for calculations, etc. It is generally not recommended this memory be used for latency critical or repetitive uses.

Table 3.20: User EEPROM (2-Wire Address A2h)

Address	# Bytes	Name	Description
128-247	120	User EEPROM	User writable EEPROM

Vendor Specific Control Function Locations [Address A2h, Bytes 248-255]

Addresses 248 – 255 are defined for vendor specific control functions. Potential usage includes proprietary functions enabled by specific vendors, often managed in combination with addresses 120-127.

Table 3.21: Vendor Control Function Addresses (2-Wire Address A2h)

Address	# Bytes	Name	Description
248-255	8	Vendor Specific	Vendor specific control functions