

Features

- Supports 9.95Gb/s to 11.1Gb/s bit rates
- Hot-pluggable XFP footprint
- Maximum link length of 10km
- Uncooled 1310nm EML/DFB laser.
- Duplex LC connector
- Power dissipation <2.5W
- Built-in digital diagnostic functions
- Temperature range -5°C to 70°C



Applications

- SONET OC-192 SR-1, SDH STM I-64.1 at 9.953Gbps
- 10GBASE-LR/LW 10G Ethernet
- 1200-SM-LL-L 10G Fibre Channel
- 10GE over G.709 at 11.09Gbps
- OC192 over FEC at 10.709Gbps

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Maximum Supply Voltage 1	Vcc3	-0.5	4.0	V
Maximum Supply Voltage 2	Vcc5	-0.5	6.0	V
Storage Temperature	TS	-40	85	°C
Case Operating Temperature	TOP	-5	70	°C

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Temperature	Top	-5		70	°C
Supply Voltage 1	Vcc3	3.13		3.45	V
Supply Voltage 2	Vcc5	4.75		5.25	V

Electrical Characteristics

(TOP = -5 to 70°C, VCC5 = 4.75 to 5.25 Volts)

Parameter	Symbol	Min.	Typ.	Max	Unit	Notes	
Main Supply Voltage	Vcc5	4.75		5.25	V		
Supply Voltage #2	Vcc3	3.13		3.45	V		
Supply Current – Vcc5 supply	Icc5			250	mA		
Supply Current – Vcc3 supply	Icc3			500	mA		
Module total power	P			2.5	W		
Transmitter							
Input differential impedance	Rin		100		Ω	1	
Differential data input swing	Vin,pp	120		820	mV		
Transmit Disable Voltage	VD	2.0		Vcc	V		
Transmit Enable Voltage	VEN	GND		GND+ 0.8	V		
Transmit Disable Assert Time				10	us		
Receiver							
Differential data output swing	Vout,pp	340	650	850	mV		
Data output rise time	tr			38	ps	2	
Data output fall time	tf			38	ps	2	
LOS Fault	V _{LOS fault}	Vcc – 0.5		VccHOST	V	3	
LOS Normal	V _{LOS norm}	GND		GND+0.5	V	3	
Power Supply Rejection	PSR	See Note 4 below					4

Notes:

1. After internal AC coupling.
2. 20 – 80 %
3. Loss Of Signal is open collector to be pulled up with a 4.7k – 10kohm resistor to 3.15 – 3.6V. Logic 0 indicates normal operation; logic 1 indicates no signal detected.
4. Per Section 2.7.1 in the XFP MSA Specification.

Optical Characteristics

(TOP = -5 to 70C, VCC5 = 4.75 to 5.25 Volts)

Parameter	Symbol	Min.	Typical	Max.	Unit
Transmitter					
Optical output Power	P	-6		0	dBm
Optical Wavelength	λ	1290		1330	nm
Optical Extinction Ratio	ER	6			dB
Sidemode Supression ratio	SSRmin			30	dB
Average Launch power of OFF transmitter	POFF	-30			dBm
Tx Jitter	Txj	Compliant with each standard requirements			
Receiver					
Receiver Sensitivity (OMA) @ 10.7Gb/s	RSENS			-14.5	dBm
Maximum Input Power	PMAX	+0.5			dBm
Optical Center Wavelength	λ_C	1270		1600	nm
Receiver Reflectance	Rrx			-14	dB
LOS De-Assert	LOSD			-18	dBm
LOS Assert	LOSA	-32			dBm
LOS Hysteresis		1			dB

Pin Descriptions

Pin	Logic	Symbol	Name/Description	Ref.
1		GND	Module Ground	1
2		VEE5	Optional -5.2 Power Supply – Not required	
3	LVTTL-I	Mod-Desel	Module De-select; When held low allows the module to , respond to 2-wire serial interface commands	
4	LVTTL-O	Interrupt	Interrupt (bar); Indicates presence of an important condition which can be read over the serial 2-wire interface	2
5	LVTTL-I	TX_DIS	Transmitter Disable; Transmitter laser source turned off	
6		VCC5	+5 Power Supply	
7		GND	Module Ground	1
8		VCC3	+3.3V Power Supply	
9		VCC3	+3.3V Power Supply	

10	LVTTTL-I	SCL	Serial 2-wire interface clock	2
11	LVTTTL-I/O	SDA	Serial 2-wire interface data line	2
12	LVTTTL-O	Mod_Abs	Module Absent; Indicates module is not present. Grounded in the module.	2
13	LVTTTL-O	Mod_NR	Module Not Ready;	2
14	LVTTTL-O	RX_LOS	Receiver Loss of Signal indicator	2
15		GND	Module Ground	1
16		GND	Module Ground	1
17	CML-O	RD-	Receiver inverted data output	
18	CML-O	RD+	Receiver non-inverted data output	
19		GND	Module Ground	1
20		VCC2	+1.8V Power Supply – Not required	
21	LVTTTL-I	P_Down/ RST	Power Down; When high, places the module in the low power stand-by mode and on the falling edge of P_Down initiates a module reset	
			Reset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle.	
22		VCC2	+1.8V Power Supply – Not required	
23		GND	Module Ground	1
24	PECL-I	RefCLK+	Reference Clock non-inverted input, AC coupled on the host board – Not required	3
25	PECL-I	RefCLK-	Reference Clock inverted input, AC coupled on the host board – Not required	3
26		GND	Module Ground	1
27		GND	Module Ground	1
28	CML-I	TD-	Transmitter inverted data input	
29	CML-I	TD+	Transmitter non-inverted data input	
30		GND	Module Ground	1

Notes:

1. Module circuit ground is isolated from module chassis ground within the module.
2. Open collector; should be pulled up with 4.7k – 10k ohms on host board to a voltage between 3.15V and 3.6V.
3. A Reference Clock input is not required .

Hostboard Connector Pinout

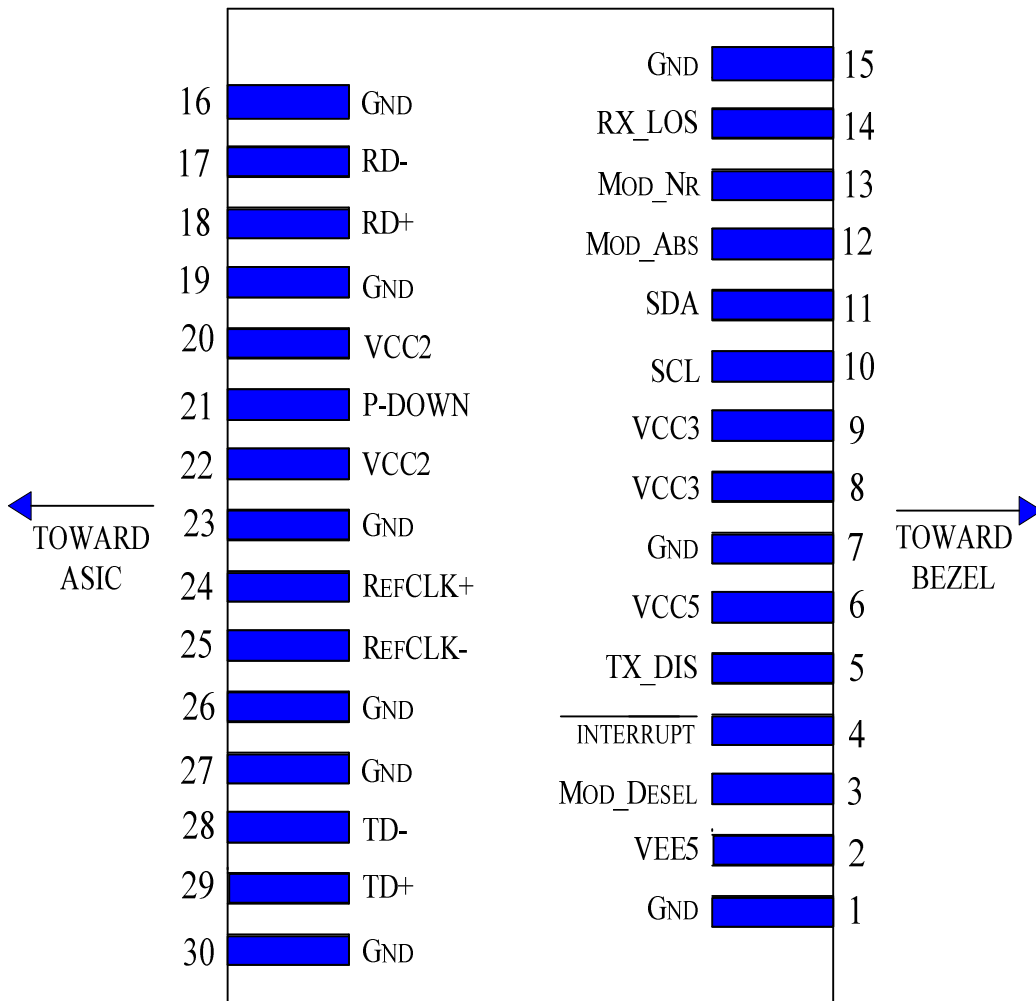


Diagram of Host Board Connector Block Pin Numbers and Name

General Specifications

Parameter	Symbol	Min	Typ	Max	Units	Ref.
Bit Rate	BR	9.95		11.1	Gb/s	1
Bit Error Ratio	BER			10 ⁻¹²		2
Max. Supported Link Length	LMAX		10		km	1

Notes:

1. SONET OC-192 SR-1, SDH STM I-64.1, 10GBASE-LR/LW, 1200-SM-LL-L
2. Tested with a 2³¹ - 1 PRBS

Digital Diagnostic Functions

SNR-XFP-LR Small Form Factor 10Gb/s (XFP) transceivers are compliant with the current XFP Multi-Source Agreement (MSA) Specification Rev 4.5.

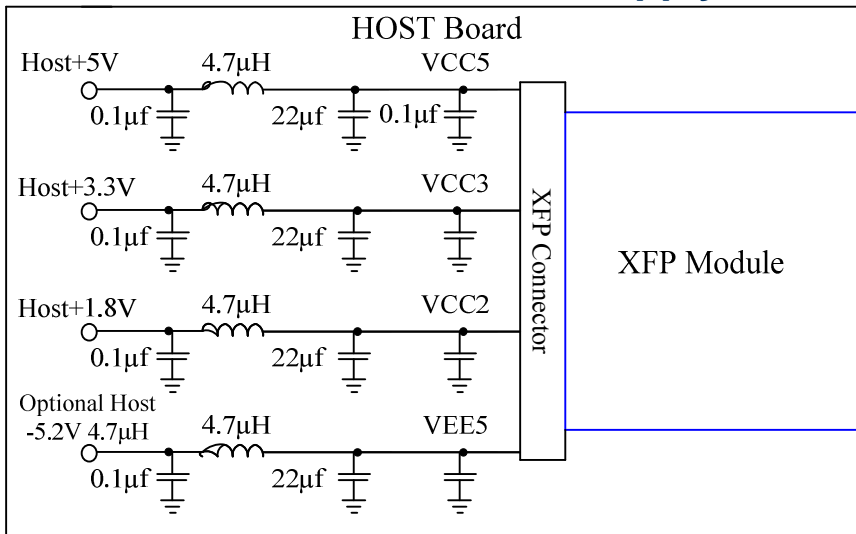
As defined by the XFP MSA, SNR's XFP transceivers provide digital diagnostic functions via a 2-wire serial interface, which allows real-time access to the following operating parameters:

- Transceiver temperature
- Laser bias current
- Transmitted optical power
- Received optical power
- Transceiver supply voltage

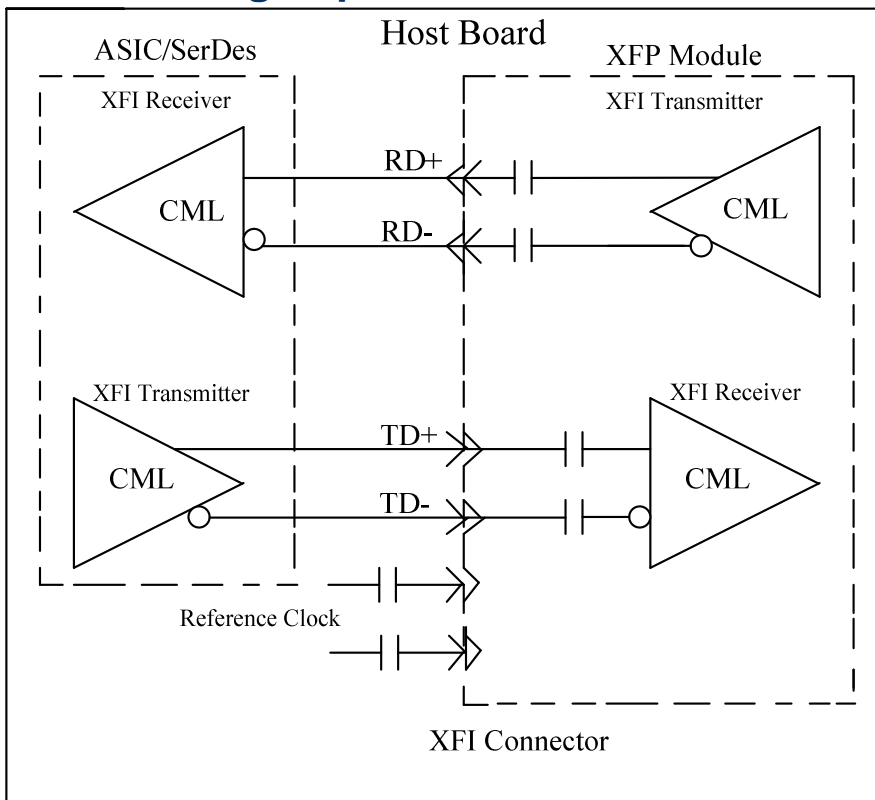
It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range.

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller inside the transceiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the XFP transceiver into those segments of its memory map that are not write-protected. The negative edge clocks data from the XFP transceiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit parameters, addressed from 000h to the maximum address of the memory.

Recommended Host Board Power Supply Circuit

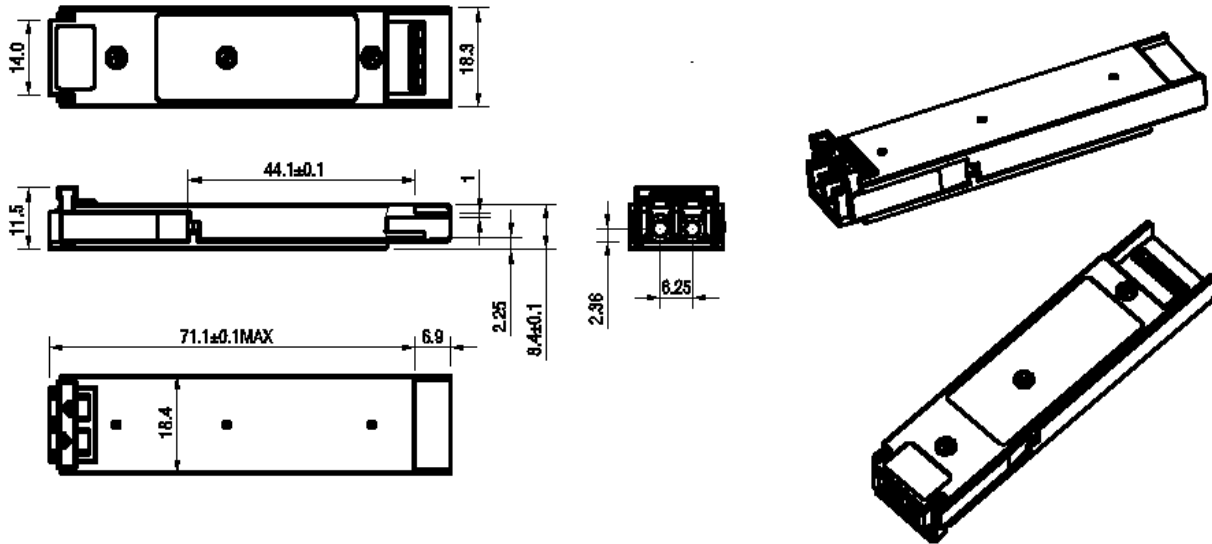


Recommended High-speed Interface Circuit



Mechanical Specifications

SNR's XFP transceivers are compliant with the dimensions defined by the XFP Multi-Sourcing Agreement (MSA).



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