

SNR-QSFP28-LR4-I

Single-Mode 100GBASE-LR4 QSFP28
Transceiver RoHS6 Compliant



Features

- ◆ Supports 103Gbps
- ◆ Single 3.3V Power Supply and Power dissipation < 3.5W
- ◆ Up to 10km over SMF
- ◆ RoHS-6 compliant (lead-free)
- ◆ Commercial case temperature range of 0°C to 70°C
- ◆ 4*25Gbps DFB-based LAN-WDM transmitter
- ◆ PIN and TIA array on the receiver side
- ◆ 4x25G electrical interface
- ◆ Duplex LC receptacles
- ◆ I²C interface with integrated Digital Diagnostic Monitoring

Applications

- ◆ 100GBASE-LR4 100G Ethernet

Ordering Information

Part No.	Data Rate	Fiber	Distance *(note2)	Interface	Temp.	DDMI
SNR-QSFP28-LR4-I*(note1)	103Gbps	SMF	10km	LC	-40°C~+85°C	Yes

Note1: Standard version

Note2: Over SMF

*The product image only for reference purpose.

Regulatory Compliance*

Product Certificate	Certificate Number	Applicable Standard
TUV	R50135086	EN 60950-1:2006+A11+A1+A12+A2
		EN 60825-1:2014
		EN 60825-2:2004+A1+A2
UL	E317337	UL 60950-1
		CSA C22.2 No. 60950-1-07
EMC CE	AE 50285865 0001	EN 55022:2010
		EN 55024:2010
FCC	WTF14F0514417E	47 CFR PART 15 OCT., 2013
FDA	/	CDRH 1040.10
ROHS	/	2011/65/EU

*The above certificate number updated to June 2014, because some certificate will be updated every year, such as FDA and ROHS. For the latest certification information, please check with LLC NAG.

Product Description

SNR-QSFP28-LR4 QSFP28 transceiver module is designed for 103Gigabit Ethernet links over 10Km single mode fiber. It is compliant with IEEE 802.3ba 100GBASE-LR4. Digital diagnostics functions are available via an I2C interface, as specified by the QSFP28 MSA.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	Ts	-40	+85	°C
Supply Voltage	Vcc	-0.5	3.6	V
Operating Relative Humidity	RH	5	85	%
Receiver Damage Threshold, per Lane	Rxdmg	5.5		dBm

*Exceeding any one of these values may damage the device permanently.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature	Tc	-40	25	85	°C
Power Supply Voltage	Vcc	3.135	3.3	3.465	V
Power Dissipation	Pd			4.8	W

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max	Unit	Notes
Transmitter						
Differential data input swing per lane				900	mV _{p-p}	
Input Impedance (Differential)	Zin			10	%	

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Stressed input parameters					
Eye width		0.46			UI
Applied pk-pk sinusoidal jitter		IEEE 802.3bm Table 88-13			
Eye height		95			mv
DC common mode voltage		-350		2850	mv
Receiver					
Differential output amplitude		200		900	mv _{p-p}
Output Impedance (Differential)	Zout			10	%
Output Rise/Fall Time	t _r /t _f	12			ps
Eye width		0.57			UI
Eye height differential		228			mv
Vertical eye closure				5.5	db

Optical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit
Transmitter					
Signaling Speed per Lane	BR _{AVE}		25.78		Gbps
Data Rate Variation		-100		+100	ppm
Lane_0 Center Wavelength	λ _{C0}	1294.53	1295.56	1296.59	nm
Lane_1 Center Wavelength	λ _{C1}	1299.02	1300.05	1301.09	nm
Lane_2 Center Wavelength	λ _{C2}	1303.54	1304.58	1305.63	nm
Lane_3 Center Wavelength	λ _{C3}	1308.09	1309.14	1310.19	nm
Total Average Output Power	P _o			10.5	dBm
Average Launch Power each Lane*(Note3)	P _{each}	-4.3		4.5	dBm
Optical Modulation Amplitude (OMA) each Lane	T _x OMA	-1.3		4.5	dBm
Difference in launch power between any two lanes (OMA)				5	dB
Launch power in OMA minus TDP, each lane		-2.3			dBm
Transmitter and dispersion penalty (TDP), each lane				2.2	dB
Extinction Ratio	ER	4			dB
Side-mode Suppression ratio	SMSR _{min}	30			dB
Average launch power of OFF transmitter per lane				-30	dBm
Relative Intensity Noise	RIN			-130	dB/hz
Transmitter Reflectance				-12	dB
Optical Return Loss Tolerance				20	dB

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Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}*(Note4)		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}			
Receiver					
Signaling Speed per Lane	BR _{AVE}		25.78		Gbps
Data Rate Variation		-100		+100	ppm
Damage threshold per lane	Rxdmg	5.5			dBm
Lane_0 Center Wavelength	λ_{C0}	1294.53	1295.56	1296.59	nm
Lane_1 Center Wavelength	λ_{C1}	1299.02	1300.05	1301.09	nm
Lane_2 Center Wavelength	λ_{C2}	1303.54	1304.58	1305.63	nm
Lane_3 Center Wavelength	λ_{C3}	1308.09	1309.14	1310.19	nm
Average Receive Power per Lane*(Note5)	Rxpow	-10.6		4.5	dBm
Receive Power (OMA) per Lane	RxOMA			4.5	dBm
Receive Sensitivity in OMA per Lane	Rxsens			-8.6	dBm
Receiver 3 dB electrical upper cutoff frequency, per lane				31	GHz
Stressed Receiver Sensitivity (OMA) per Lane*(Note6)	RX _{SRS}			-6.8	dBm
Optical Return Loss	ORL			-26	dB
LOS Assert	LOSA	-25			dBm
LOS De-Assert	LOSD			-12	dBm
LOS Hysteresis		0.5			dB
Conditions of stressed receiver sensitivity test					
Vertical eye closure penalty*(Note7)	VECP		1.8		dB
Stressed eye J2 Jitter*(Note7)	J2		0.3		UI
Stressed eye J9 Jitter*(Note7)	J9		0.47		UI

Note3: Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

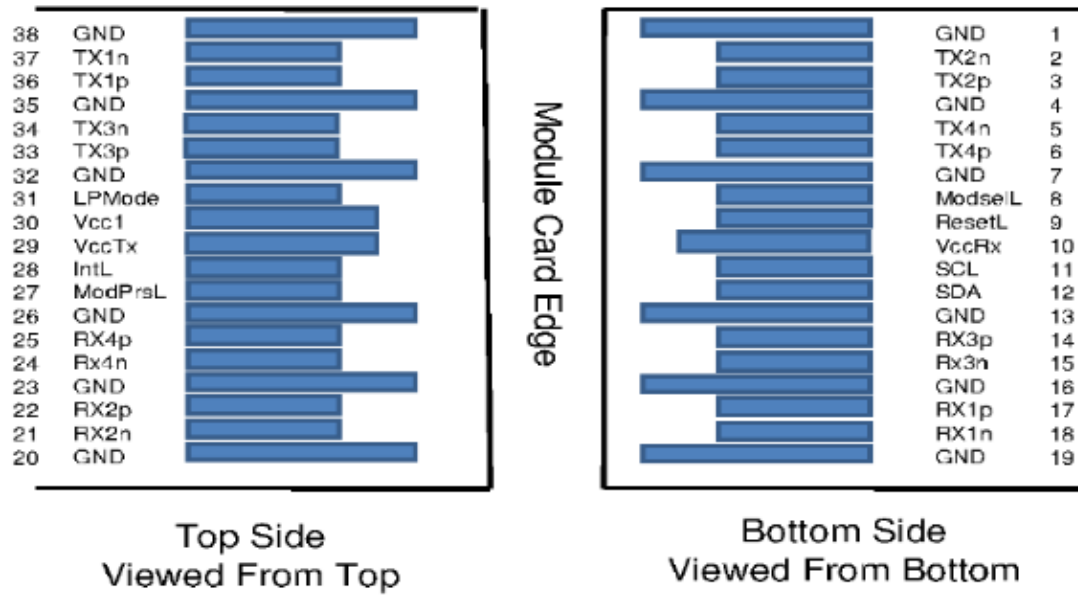
Note4: Hit ratio 5×10^{-5} .

Note5: Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

Note6: Measured with conformance test signal at TP3 for BER = 10–12.

Note7: Vertical eye closure penalty, stressed eye J2 Jitter, and stressed eye J9 Jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

QSFP28 Transceiver Electrical Pad Layout



Pin Arrangement and Definition

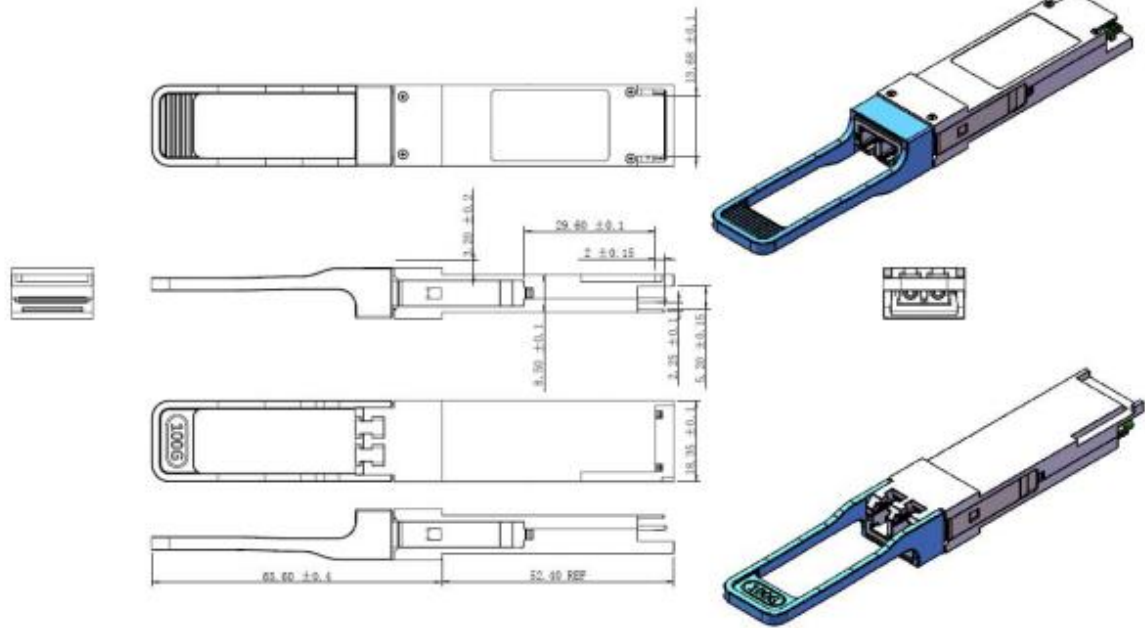
Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		VccRx	+3.3V Power Supply Receiver	2	2
11	LVCMOS- I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS- I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	

22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTTL-O	ModPrsL	Module Present	3	
28	LVTTTL-O	IntL	Interrupt	3	
29		VccTx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTTL-I	LPMODE	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

1: GND is the symbol for signal and supply (power) common for the QSFP28 module. All are common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table 6. Recommended host board power supply filtering is shown in Figures 3 and 4. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP28 Module in any combination. The connector pins are each rated for a maximum current of 500Ma.

Mechanical Specifications



*This 2D drawing only for reference, please check with LLC NAG before ordering.

GUARANTEE:



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