Catalyst 9600

You make networking **possible**

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Cisco Catalyst 9600 Series Switches

Cisco Catalyst 9600 Series
Chassis

Dual-serviceable fan tray

Built-in RFID

Blue Beacons (system/fan tray, sup, line cards)

Modular power supplies

4 line card slots

2 supervisor slots (dedicated)

6.4 Tbps per slot from each supervisor slot

Dimensions (HxWxD inches) 13.95 x 17.4 x 16.1 (8RU)

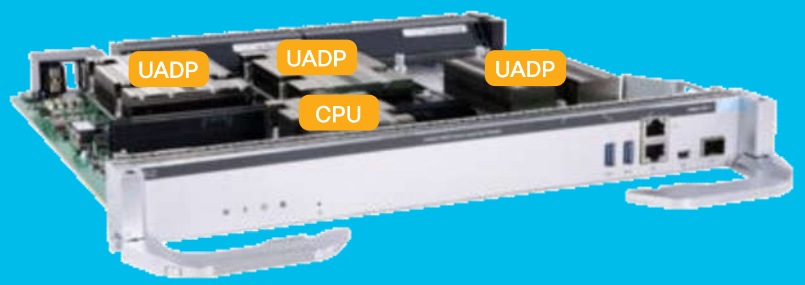
Cisco Catalyst 9600 Series
C9606R chassis port density

Port speed	Density with supervisor 1	Maximum chassis density
100G	48	128
40G	96	128
25G	192	192
10G	192	192
1G*	192	192

Line Rate non-blocking

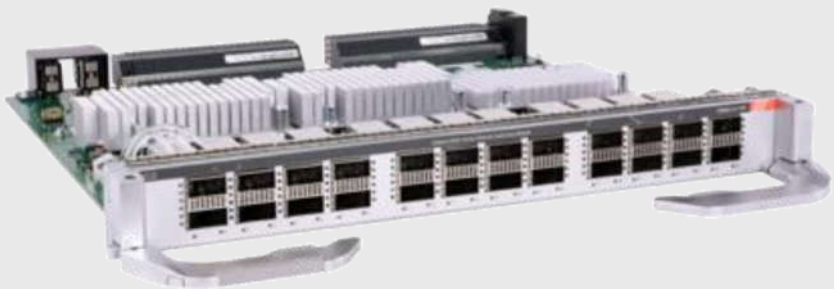
*Roadmap

Cisco Catalyst 9600 Series
Supervisor 1



9.6 Tbps	2.4 Tbps per slot
3x UADP 3.0 ASIC	**8 core** X86 CPU @2.0 Ghz
M.2 SATA SSD (optional: up to 1 TB)	16G DDR4 memory
Built-in RFID	Mgmt ports: copper and **fiber**
Blue Beacon	2x USB3 1x mini-B USB console

Cisco Catalyst 9600 Series
Line cards

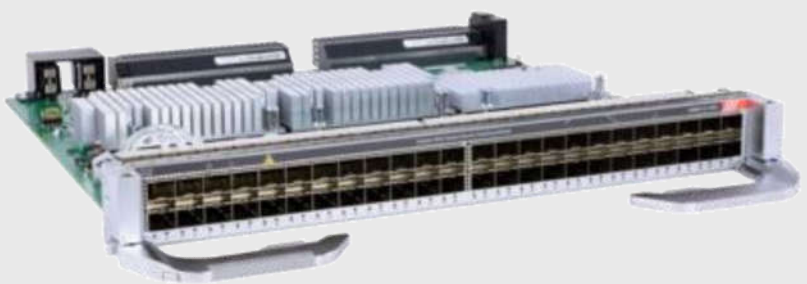


C9600-LC-24C - 100G/40G (fiber)

- 24 ports
- QSFP28/QSFP+
- Supports 100G and 40G

C9600-LC-48YL - 25G/10G/1G* (fiber)

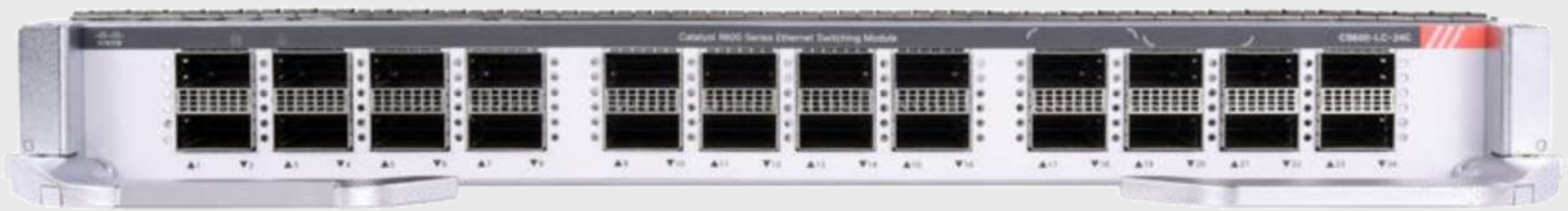
- 48 ports
- SFP28/SFP+/SFP
- Supports 25G, 10G, and 1G



*Roadmap

The Y in the product ID (PID) indicates the hardware capability

Cisco Catalyst 9600 Series
100G/40G Line card - C9600-LC-24C

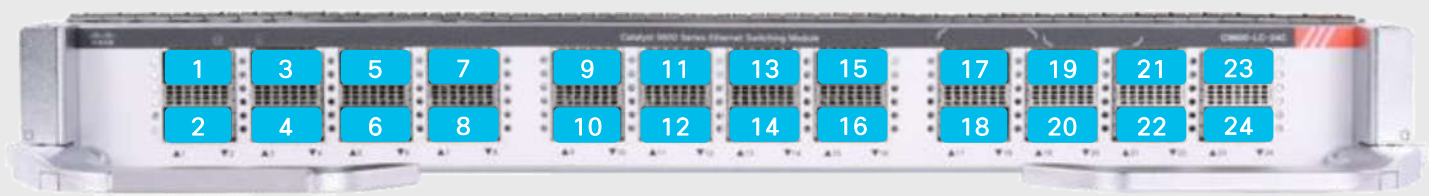


- All 24 ports are capable of 100G (QSFP28)/40G (QSFP+)
- Hardware-ready with QSA (for 1G/10G)
- With Supervisor Engine 1
  - 100G: Every 2 ports in a port-group. The odd number of ports can be 100G and the next even number port is disabled. (Maximum of 12x 100G, line rate with 187 byte or higher)
  - 40G - 24x 40G (line rate with 148 byte or higher)

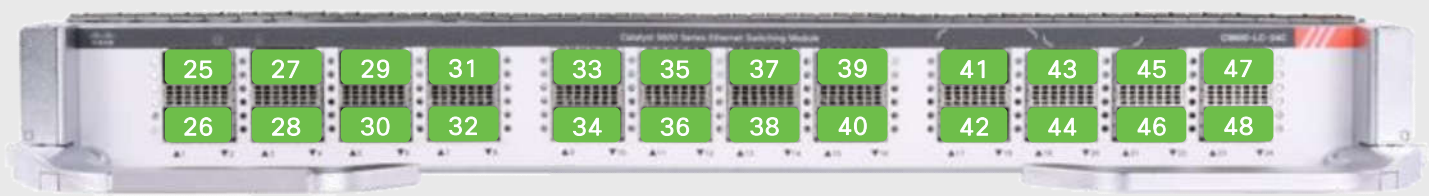
C9600-LC-24C – Port Numbering with Supervisor Engine 1

- 40G numbering from 1 to 24
- 100G number from 25 to 48

40G port numbering



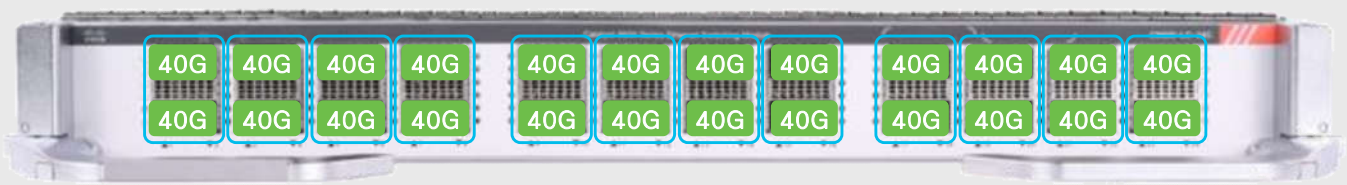
100G port numbering



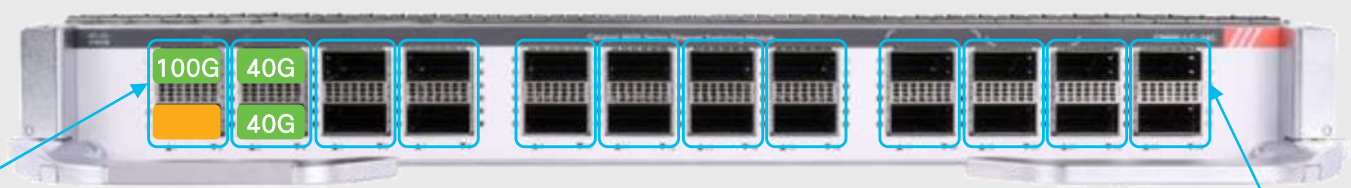
C9600-LC-24C with supervisor engine 1

- This line card appears in 40G mode by default
- Future supervisors can support 100G speed on all ports at the same time

Default mode
(all ports 40G)



100G
configuration



Fo<slot#>/0/1
Hu <slot#>/0/25

interface HundredGigE1/0/25 enable

- Enable Hu1/0/25 as 100G
- Disabled Fo1/0/1 and 1/0/2

Fo<slot#>/0/23
Hu <slot#>/0/47

Cisco Catalyst 9600 Series
25G/10G/1G Line card – C9600-LC-48YL

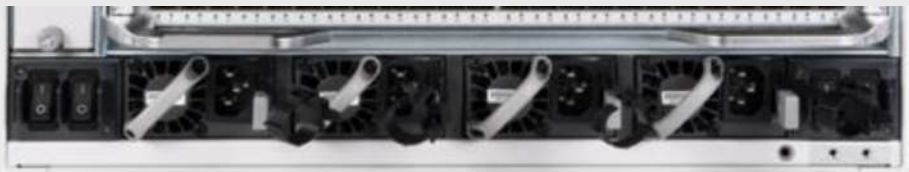
- All 48 ports support 25G/10G/1G
- Hardware capable of 10/100M
- Line rate with 25G/10G/1G (at 187 bytes for 25G; any packet size with 10G/1G)
- Any port, any supported speed
- Port reference is always ”TwentyFive<slot#>/0/<port#>” and port speed is auto-detected based on the inserted transceiver

Cisco Catalyst 9600 Series
Fan tray

- N+1 (8+1) fan redundancy
- Flexible service - fan tray can be replaced from the portside or the back
- Efficient - variable speed per fan depends on the load, temperature, and altitudes (=>lower noise)
- Airflow – side-to-side airflow

Fan tray hot-swappable needs to be done within 120 seconds

Cisco Catalyst 9600 Series
Power supplies

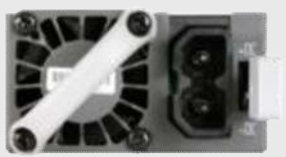


- Chassis has 4 slots for power supply
- Individual on/off switch for each power supply
- Supports a mix of AC (@220V) and DC power supplies

AC

- Supports both 110V and 220V input
- 2 KW output with 220V (1050W with 110V)
- Platinum rate power supply
- Redundant mode: Combined and N+1

DC



- Supports input range of -40V to -72V
- 2 KW output
- Platinum rate power supply
- Redundant mode: Combined and N+1

Architecture

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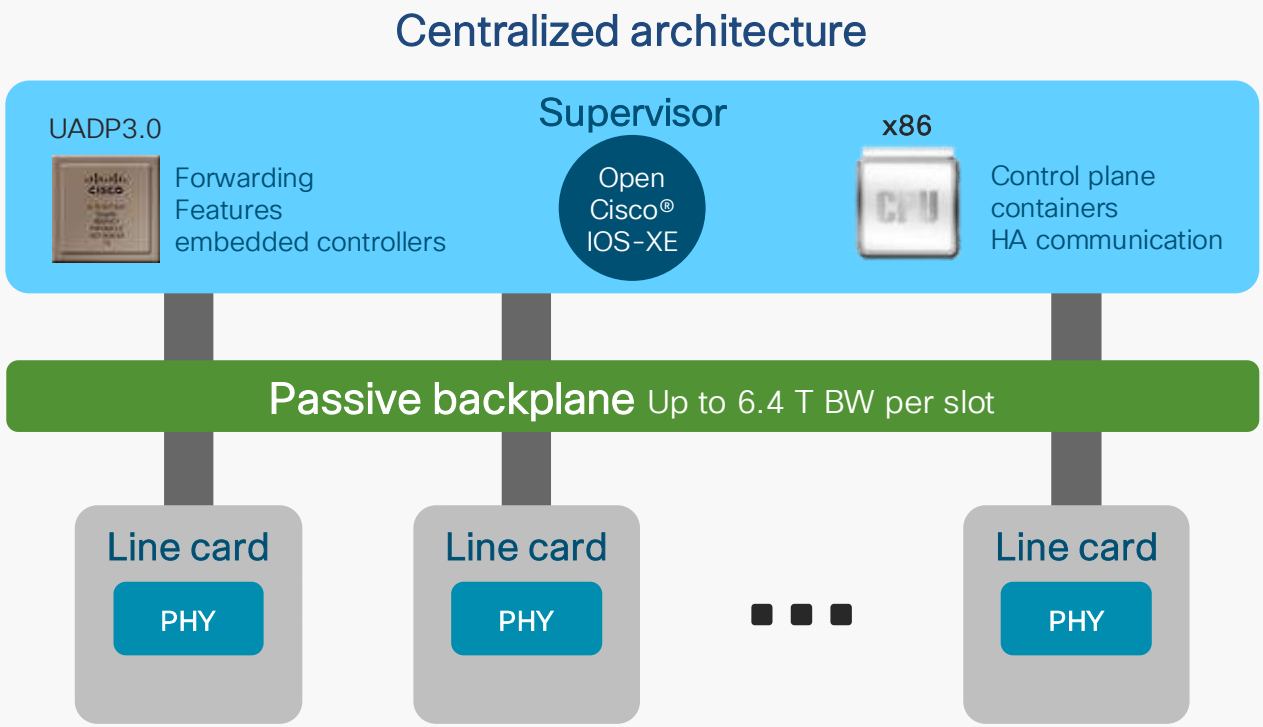
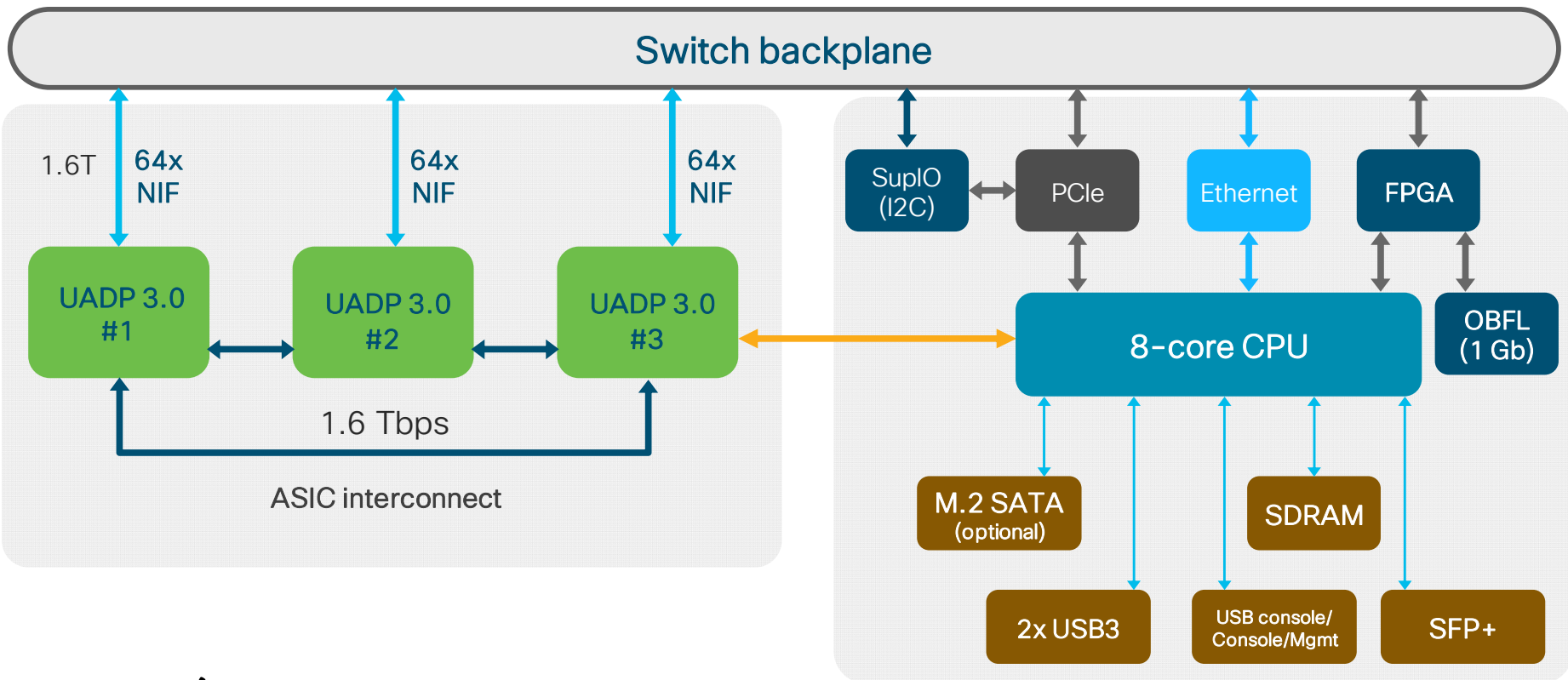
Architecture

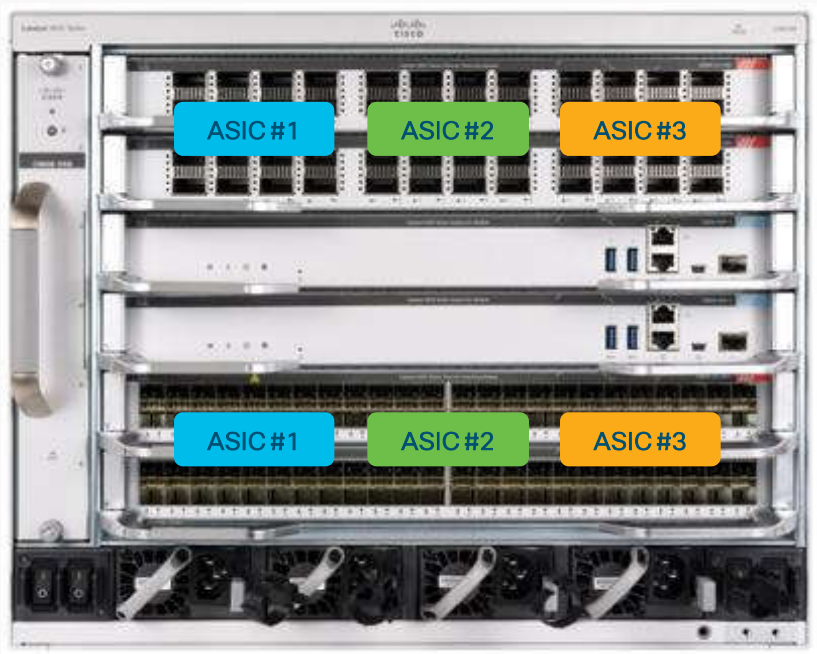


- Centralized architecture => **Uninterrupted supervisor switchover**
- Centralized architecture (Forwarding, queuing, and security are done on the supervisor) => **Unlock new capability** with a supervisor upgrade
- Transparent line cards => **Compatible** with new sup
- Passive backplane => **High MTBF**
- X86 CPU + storage => **App hosting**

Supervisor engine 1 – Block diagram



Supervisor engine 1 – ASICs to LC mapping



- ASIC #1: First third of the ports
  - 48-port module: 1-16
  - 24-port module: 1-8
- ASIC #2: Middle third of the ports
  - 48-port module: 17-32
  - 24-port module: 9-16
- ASIC #3: Last third of the ports
  - 48-port module: 33-48
  - 24-port module: 17-24

Cisco Catalyst 9600 – Supervisor 1
Port-to-ASIC mapping

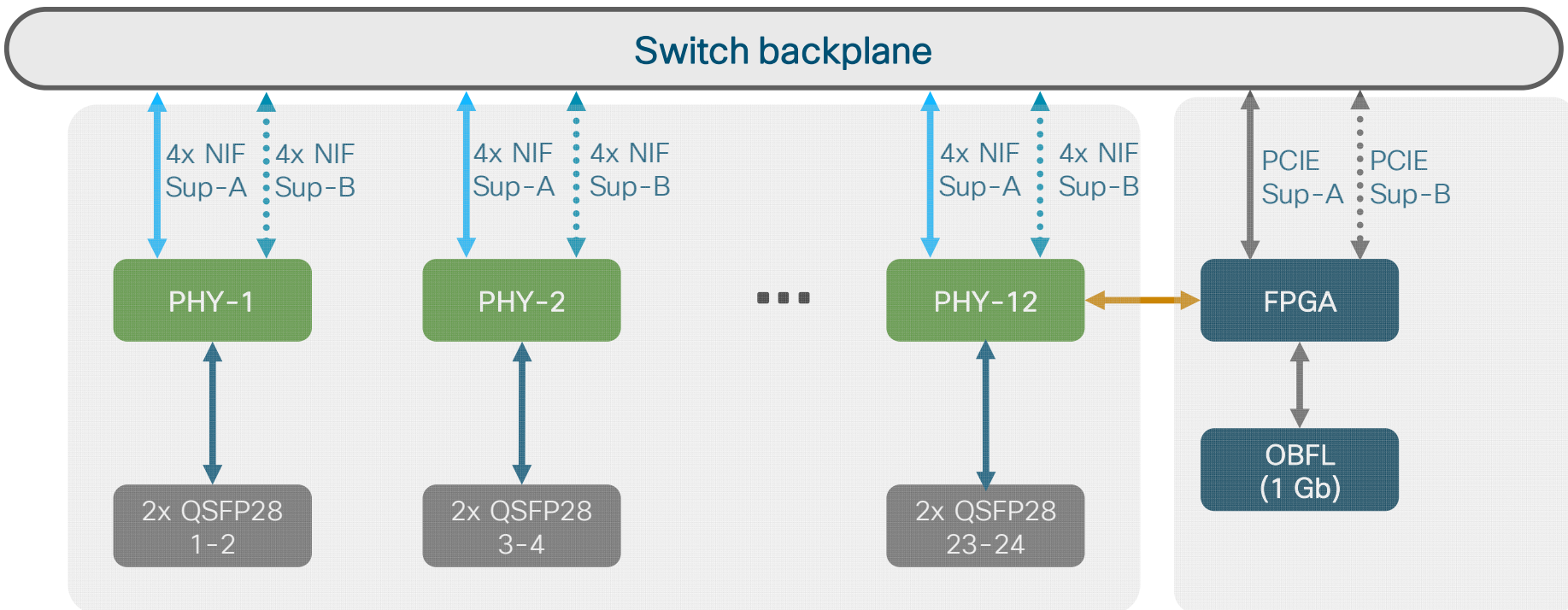
Reference

Command to verify the port-to-ASIC mapping:
show platform software fed active ifm mappings

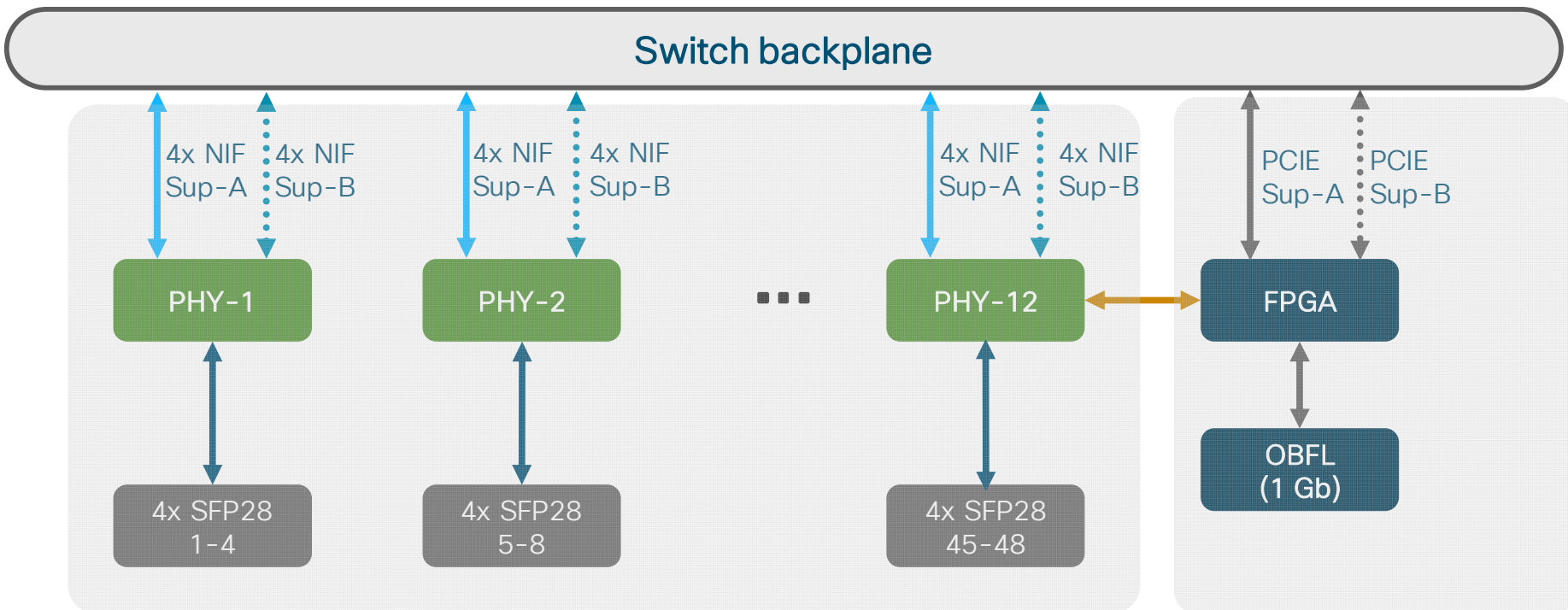
```
C9600-Bottom#show platform software fed active ifm mappings
Interface                IF_ID    Inst Asic Core Port SubPort Mac  Cntx LPN  GPN  Type Active
FortyGigabitEthernet1/0/1 0x7       0   0    0    0      0      0    0    1    101  NIF  N
FortyGigabitEthernet1/0/2 0x8       0   0    0    8      0      2    1    2    102  NIF  N
FortyGigabitEthernet1/0/3 0x9       0   0    0    16     0      16   0    3    103  NIF  N
FortyGigabitEthernet1/0/4 0xa       0   0    0    24     0      18   1    4    104  NIF  N
FortyGigabitEthernet1/0/5 0xb       1   0    1    8      0      14   1    5    105  NIF  Y
FortyGigabitEthernet1/0/6 0xc       1   0    1    0      0      12   0    6    106  NIF  Y
FortyGigabitEthernet1/0/7 0xd       1   0    1    24     0      30   1    7    107  NIF  Y
FortyGigabitEthernet1/0/8 0xe       1   0    1    16     0      28   0    8    108  NIF  Y
FortyGigabitEthernet1/0/9 0xf       2   1    0    0      0      0    0    9    109  NIF  Y
<SNIP>
FortyGigabitEthernet1/0/16 0x16      3   1    1    16     0      28   0    16   116  NIF  Y
FortyGigabitEthernet1/0/17 0x17      4   2    0    0      0      0    0    17   117  NIF  Y
<SNIP>
FortyGigabitEthernet1/0/24 0x1e      5   2    1    16     0      28   0    24   124  NIF  N
HundredGigE1/0/25        0x1f      0   0    0    0      0      0    0    25   125  NIF  Y
<SNIP>

C9600-Bottom#$
```

100G/40G line card block diagram



25G/10G/1G line card block diagram



Cisco Catalyst 9600 Series – Supervisor engine 1
Switch Database Management (SDM) template

Core template
Maximizes system resources for Layer 3 unicast and multicast **routes (default)**

SD-Access template
Maximizes system resources for **policy** to support **fabric** deployment

User-customizable template
Allows customizable ACL TCAM resources

Cisco® Catalyst® 9600 Series

Distribution template
Balances system resources between Layer 3 **routes** and Layer 2 **MAC** and **Netflow**

NAT template
Maximizes the **NAT** configurations on the switch

Cisco Catalyst 9600 Series

SDM templates and scale numbers

Feature		Distribution template	Core template (default)	SDA template	NAT template
Routes (IPv4/IPv6)		114K/114K	212K/212K	212K/212K	212K/212K
Multicast routes (IPv4/IPv6)		16K/16K	32K/32K	32K/32K	32K/32K
MAC address table		82K	32K	32K	32K
Flexible NetFlow		98K/ASIC	64K/ASIC	64K/ASIC	64K/ASIC
SGT label		32K	32K	32K	32K
Security ACL	Ingress	12K		8K	12K
	Egress	15K		19K	8K
QOS ACL	Ingress	8K		8K	4K
	Egress	8K		8K	4K
NetFlow ACL	Ingress	1K		1K	1K
	Egress	1K		1K	1K
SPAN	Ingress	0.5K		0.5K	0.5K
	Egress	0.5K		0.5K	0.5K
PBR/NAT		3K		2K	15.5K
CPP		1K		1K	1K
Tunnel termination and MACsec		3K		3K	2K
LISP		1K		2K	1K

Customizable ACL TCAM resources

Cisco Catalyst 9600 Series
SDM template – Customizable TCAM section

C9600-Bottom#sho sdm prefer
Showing SDM Template Info

This is the Core template.

Security Ingress IPv4 Access Control Entries*	:	6656 (current) - 6656 (proposed)
Security Ingress Non-IPv4 Access Control Entries*	:	5632 (current) - 5632 (proposed)
Security Egress IPv4 Access Control Entries*	:	6656 (current) - 6656 (proposed)
Security Egress Non-IPv4 Access Control Entries*	:	8704 (current) - 8704 (proposed)
QoS Ingress IPv4 Access Control Entries*	:	4608 (current) - 4608 (proposed)
QoS Ingress Non-IPv4 Access Control Entries*	:	3584 (current) - 3584 (proposed)
QoS Egress IPv4 Access Control Entries*	:	4608 (current) - 4608 (proposed)
QoS Egress Non-IPv4 Access Control Entries*	:	3584 (current) - 3584 (proposed)
Netflow Input Access Control Entries*	:	1024 (current) –1024 (proposed)
Netflow Output Access Control Entries*	:	1024 (current) – 1024 (proposed)
Flow SPAN Input Access Control Entries*	:	512 (current) – 512 (proposed)
Flow SPAN Output Access Control Entries*	:	512 (current) – 512 (proposed)

Cisco Catalyst 9600 Series
SDM customizable template – CLI

Customizable range: 10% - 90%

- Between input and output
- Between IPv4 and non-IPv4

Security-ACL allocation	Default	
27K	12K (input)	7K (v4)
		5K (non-v4)
	15K (output)	7K (v4)
		8K (non-v4)

Example 1

Security-ACL allocation	Input =10% Input V4 – 75% Output v4 – 75%	
27K	3K (input)	2K (v4)
		1K (non-v4)
	24K (output)	18K (v4)
		6K (non-v4)

Example 2

Security-ACL allocation	Input = 50% Input V4 – 75% Output v4 – 75%	
27K	13K (input)	9.5K (v4)
		3.5K (non-v4)
	14K (output)	10.5K (v4)
		3.5K (non-v4)

Example 3

Security-ACL allocation	Input = 90% Input V4 – 75% Output v4 – 75%	
27K	24K (input)	18K (v4)
		6K (v4)
	3K (output)	2K (v4)
		1K (non-v4)

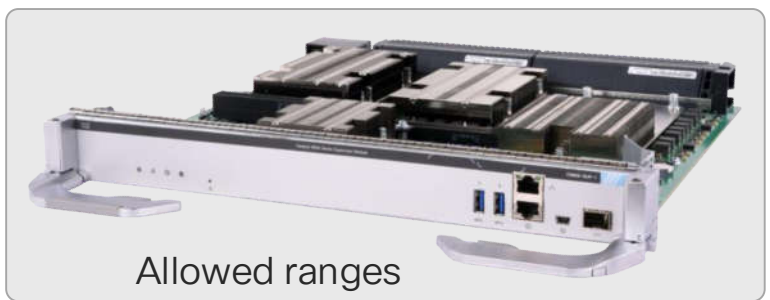
Cisco Catalyst 9600 Series – Supervisor Engine 1

SDM customizable template – CLI

Reference

Command to modify ACL TCAM allocation

```
C9600(config)#sdm prefer template-modification?
  default       Default prefered template
  fspan         Filter Span
  nfl           NFL ACLs
  qos           QOS
  security-acl  Security ACLs
```




```
C9600 (config)# sdm prefer template-modification security-acl input allowed-range
Total_size: 27648 Suggested split percentage for input: 11 18 22 25 33 37 40 48 49 52 60 63 67 75 78 82 89
```

```
C9600(config)#sdm prefer template-modification security-acl input 15 input-ipv4 15 output-ipv4 85
Allocated Security Acl Input (IPv4:1024, Non-IPv4:4096) entries, Output (IPv4:18432, Non-IPv4:4096) entries
input=18.52 input_ipv4=20.00, output_ipv4=81.82
Modifications to the preferred template have been stored, but cannot take effect until the next reload. Allocations will be an approximation of user-specified percentages. Use 'show sdm prefer' to see proposed values.

C9600(config)#
```

Catalyst 9600 Design Consideration

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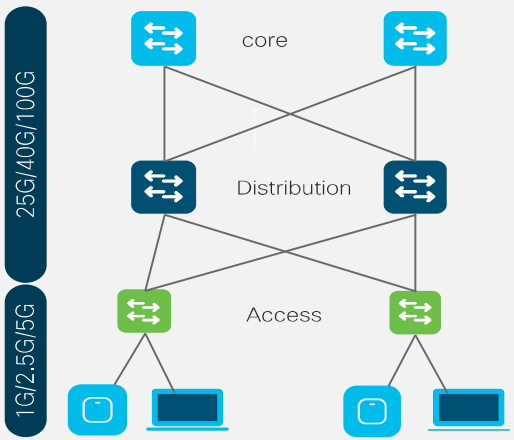
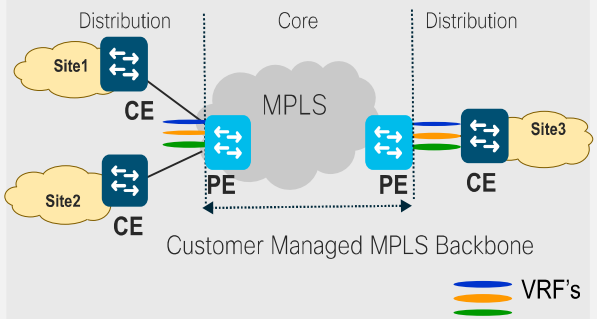
Catalyst 9600 for Multidomain Campus Core

L3/Collapsed Core



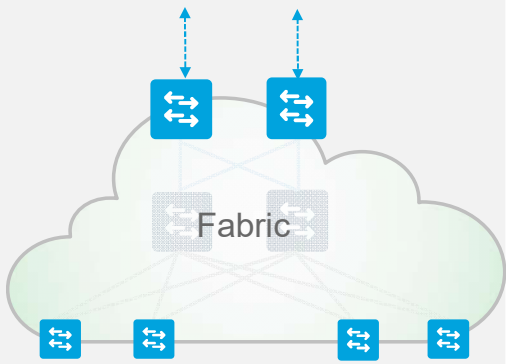
- Reduced Complexity, Resiliency & Scale
- IPv4/IPv6, Unicast & Multicast, QoS & ACL Scale

L3 Core + MPLS PE



- Segmentation, Scale, LAN/WAN Consistency
- MPLS VPNs (L2 & L3), MPLS over GRE

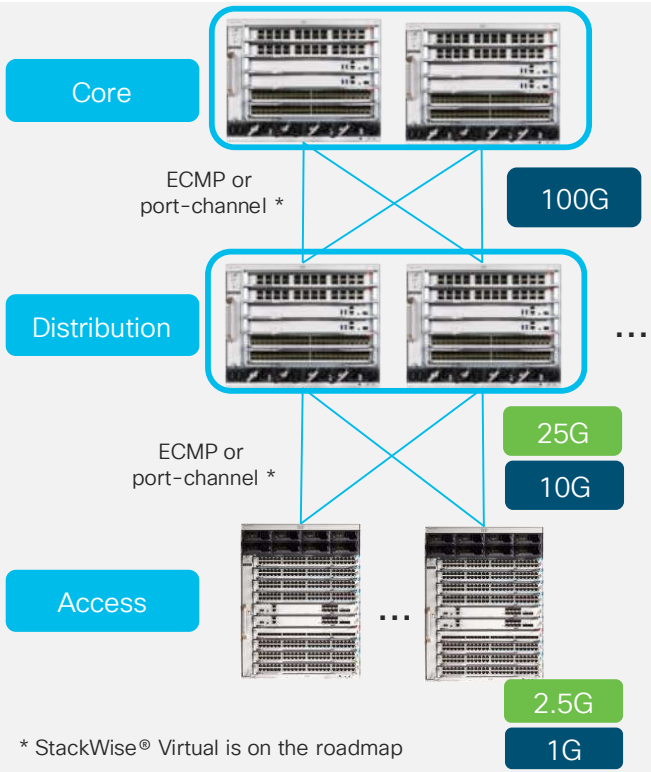
Fabric Border



- Segmentation & Automation/Programmability
- Turnkey Solution: SD-Access
- DIY : BGP EVPN VxLAN

One Platform. Any Place. Any Speed (1G to 100G)

Example of a Traditional Three-Tiers Campus Design



- Catalyst® 9606R Switch with 4x C9600-LC-24C for connection to the distribution layer, WAN, and between core devices
- Oversubscription ratio of 4:1 from distribution to core

Core

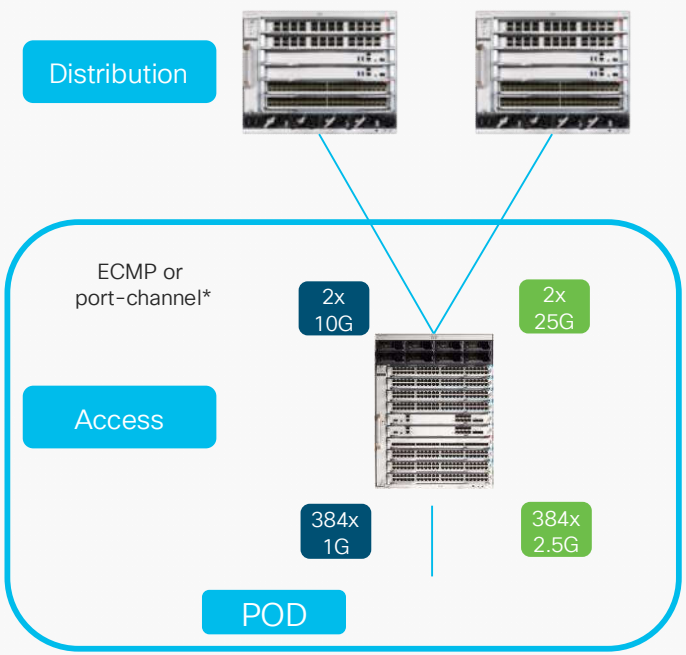
- Catalyst 9606R with 1x C9606-LC-24C as the uplink connection to the core and 3x C9606-LC-48YL as the downlink connection to the access layer
- Oversubscription ratio of 20:1 from access to distribution

Distribution

- Catalyst 9410 with 1G copper and/or mGig modules with Sup1-XL-Y
- 8x Catalyst 9300 StackWise-480 with 10G/25G uplinks

Access

Access Layer – POD



* StackWise® Virtual is on the roadmap

Cisco® Catalyst® 9400

- A Catalyst 9410 switch provides a total of 384 ports of 1G
- Catalyst 9410 can also provide 192x1G + 192x mGig ports (up to 10G)

Catalyst 9300 StackWise®-480

- Stack of 8 can provide a total of 384 ports of 1G or 2.5G (mGig)
- Stack of 8 can also provide 384 ports of 1G and mGig combination

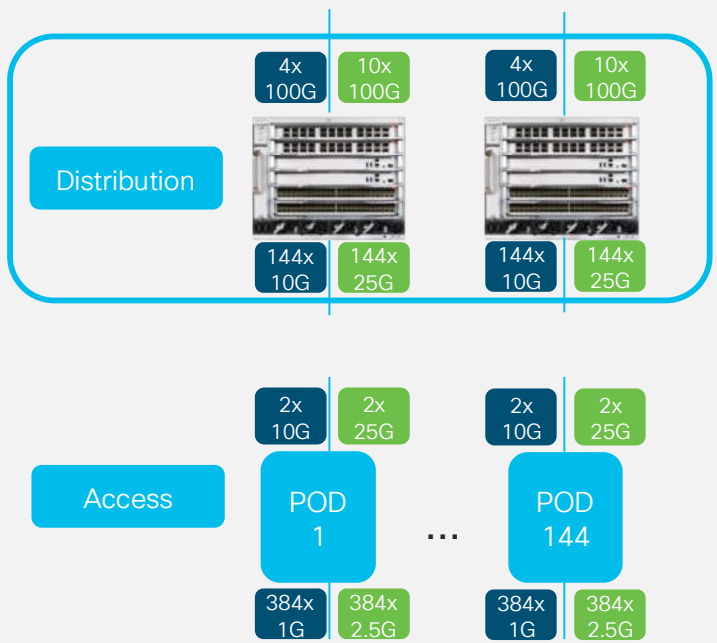
Aggregated downlink BW:

- 384G with 384x 1G
- 960G with 384x 2.5G

Uplinks BW needed for 20:1 oversubscription from access to distribution

- 2x 10G for 384x 1G
- 2x 25G for 384x 2.5G

Distribution Layer – Block



* StackWise® Virtual is on the roadmap

Cisco® Catalyst® 9606R Switch Downlinks:

- 3x C9600-LC-48YL per Catalyst 9606R
- A total of 144 x 10G/25G ports per chassis
- Aggregate downlink BW per Catalyst 9606 Switch
  1. With 10G uplinks: 144x 10G = 1.44T
  2. With 25G uplinks: 144x 25G = 3.6T

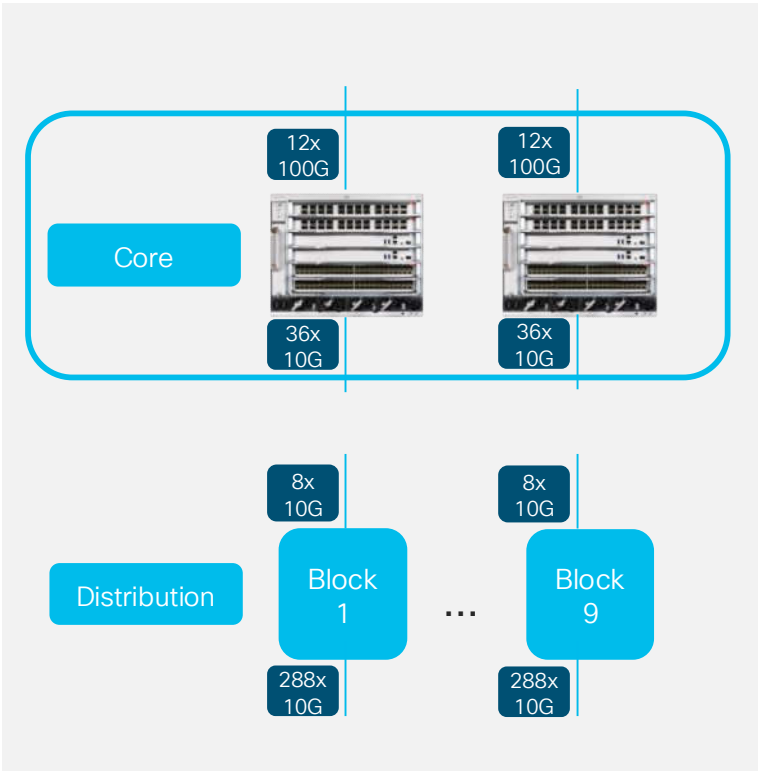
Uplinks

- 1x C9606-LC-24C per Catalyst 9606R
- To maintain 4:1 oversubscription between distribution and core layers
  1. With 10G uplinks: BW = 1.44T/4 = 360G => 4x 100G ports
  2. With 25G uplinks: BW = 3.6T/4 = 900G => 10x 100G ports

(The remaining 100G/40G ports can be used for ECMP or StackWise Virtual when it is available.)

Each distribution block can aggregate 144 access PODs.
That's 144 x 384 = **55,296** of 1G, or 2.5G ports

Core Layer with 1G in the Access Layer



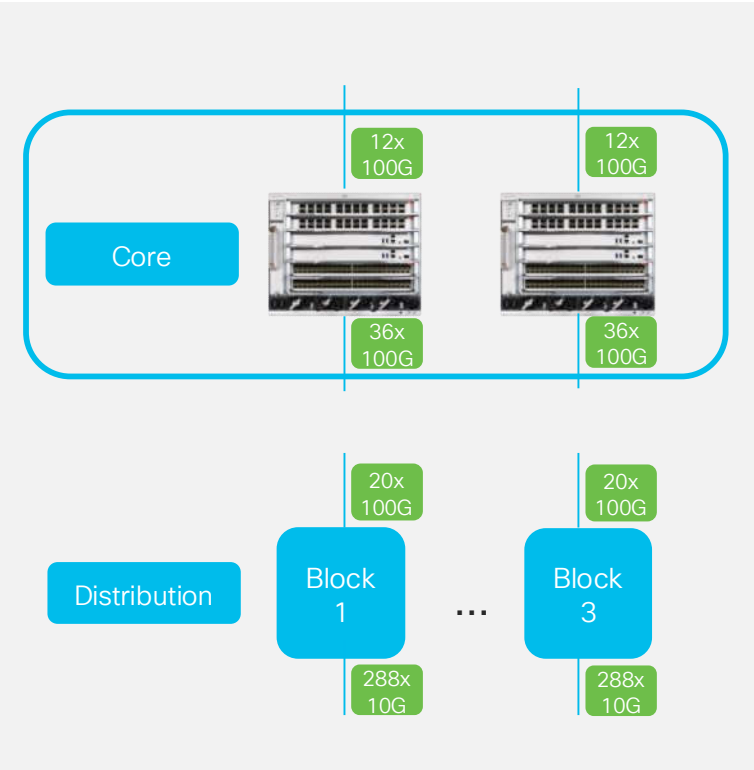
Cisco® Catalyst® 9606R Switch

- 4x C9606-LC-24C
  - 75% of ports (36x 100G) to distribution
  - 25% of ports (12x 100G) for connections between the two cores and the WAN
- Two of the core devices will provide 72x 100G for the distribution layer

- 1G aggregation
  - With 8x 100G per distribution block, two Catalyst 9606R Switches with the above configuration can aggregate 72/8, or 9 distribution blocks

The total number of 1G ports:
9x 144 x 384 = **497,664** of 1G ports

Core Layer with 2.5G in the Access Layer



Cisco® Catalyst® 9606R Switch

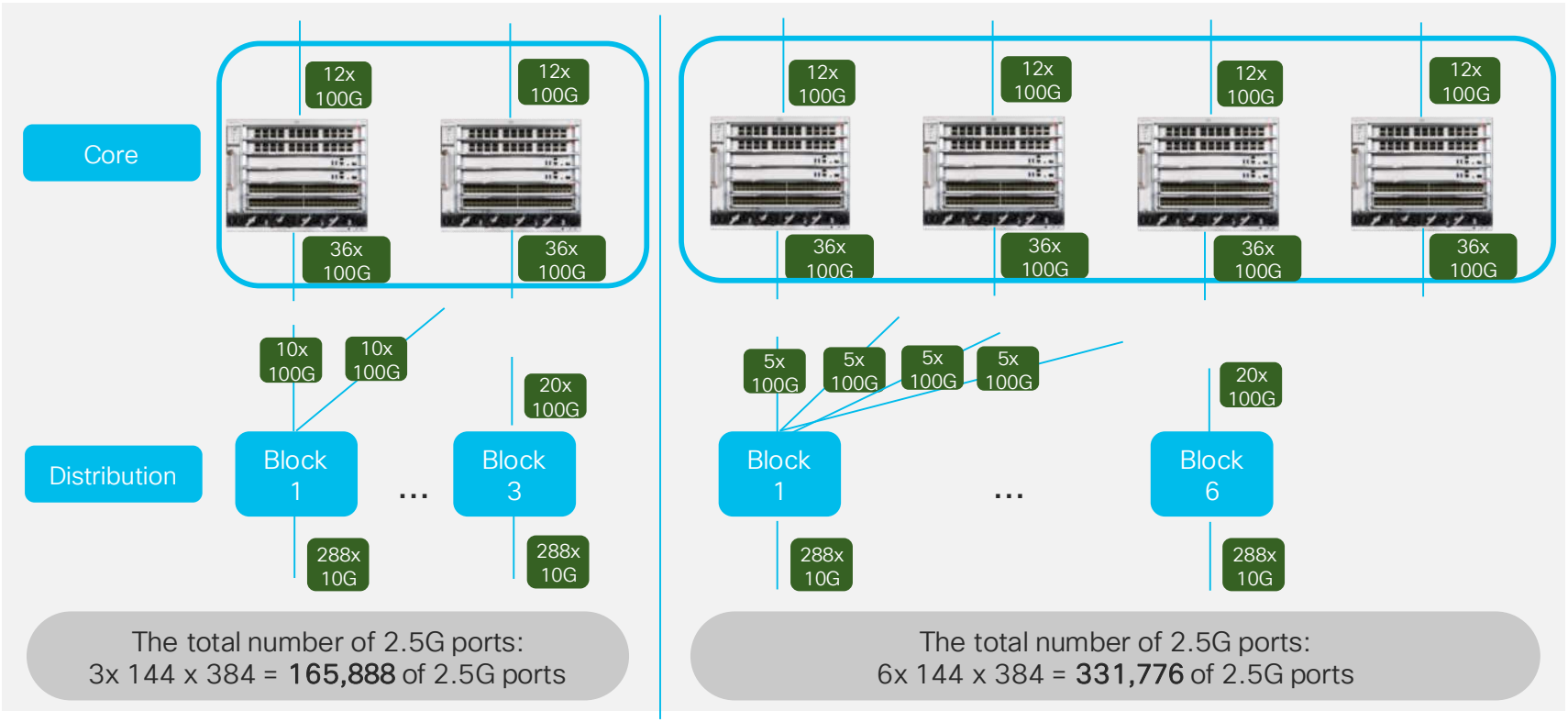
- 4x C9606-LC-24C
  - 75% of ports (36x 100G) to distribution
  - 25% of ports (12x 100G) for connections between the two cores and the WAN
- Two of the core devices will provide 72x 100G for the distribution layer

- 2.5G aggregation
  - With 20x 100G per distribution block, two of Catalyst 9606R Switches with the above configuration can aggregate 72/20, or 3 distribution blocks

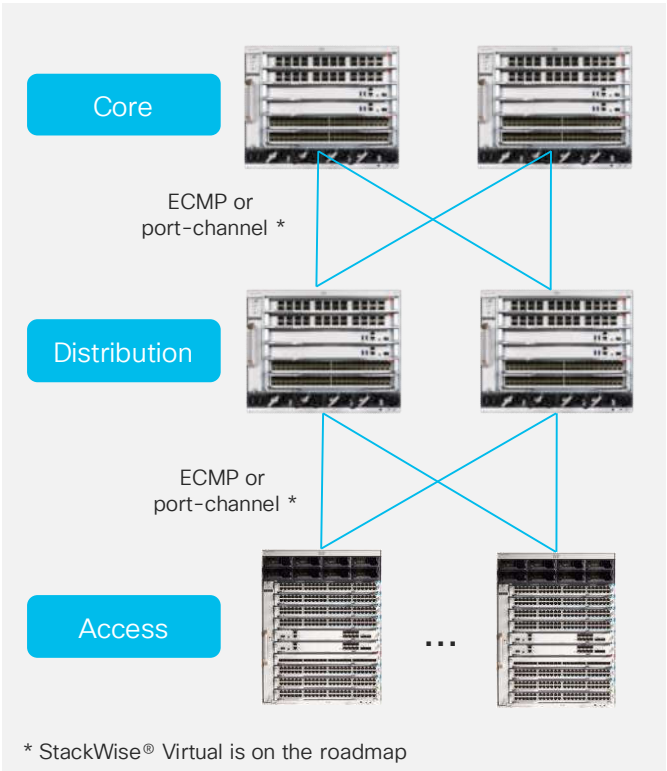
The total number of 2.5G ports:
3x 144 x 384 = **165,888** of 2.5G ports

Core Layer with 2.5G in the Access Layer

With 4x Catalyst 9606 in the core



Summary



Two Cisco Catalyst 9606R Switches in the core can provide:

1. 497K of 1G ports, or
2. 165K of 2.5G ports

Oversubscription = 4:1		
Uplinks (40/100G module):	4x 100G	10x 100G
Downlinks (10/25G modules):	144x 10G	144x 25G

Oversubscription: 20:1		
Uplinks (Supervisor or uplink module):	2x 10G	2x 25G
Downlinks (1G/mGIG module):	384x 1G	384x 2.5G