

SNR-QSFP56-SR4

OSFP 2xFR4 Series

SNR-QSFP56-SR4

Multi-Mode, 200G, QSFP56

With MPO12 interface

Features

- ◆ Supports 212.5Gbps
- ◆ Single 3.3V power supply
- ◆ Power dissipation: Commercial version < 5W
- ◆ Up to 100m OM4 and 70m over OM3
- ◆ 4x26.5625GBd (PAM4) electrical interface
- ◆ MPO-12 connector
- ◆ Commercial case temperature range of 0°C to 70°C
- ◆ VCSEL transmitter
- ◆ PIN and TIA array on the receiver side
- ◆ Loopback not Supported
- ◆ I2C interface with integrated Digital Diagnostic Monitoring
- ◆ Safety certification: TUV/UL/FDA*1
- ◆ RoHS compliant (lead-free)

Applications

- ◆ 200G SR4 applications

Ordering information

Part No.	Data Rate	Fiber Type	Distance	Optical Interface	Temp.	Management
SNR-QSFP56-SR4 ^{note2}	212.5Gbps	OM4/ OM3	100m/ 70m	MPO12 APC	0~+70°C	SFF-8636
SNR-QSFP56-SR4-I	212.5Gbps	OM4/ OM3	100m/ 70m	MPO12 PC	0~+70°C	SFF-8636

Note1: For the latest certification information, please check with NAG.

Note2: Over SMF

Product Description

SNR QSFP56 200G transceiver module is designed for use in 200 Gigabit Ethernet links up to 100m over OM4 and 70m over OM3 multi-mode fiber. The module has 4 independent electrical input/output channels operating at 53.125Gbp/s per channel. This transceiver consists of a transmitter/receiver unit operating on 850nm wavelength. The transmitter path of the module incorporates a PAM4 re-timer ASIC integrated with a 4-channel modulators driver, 4 externally modulated lasers. On the receiver path, there are 4 photodiodes and one 4-channel linear TIA arrays, along with the PAM4 re-timer. The electrical interface of the module is compliant with the 200GAUI-4 interface as defined by IEEE 802.3bs.

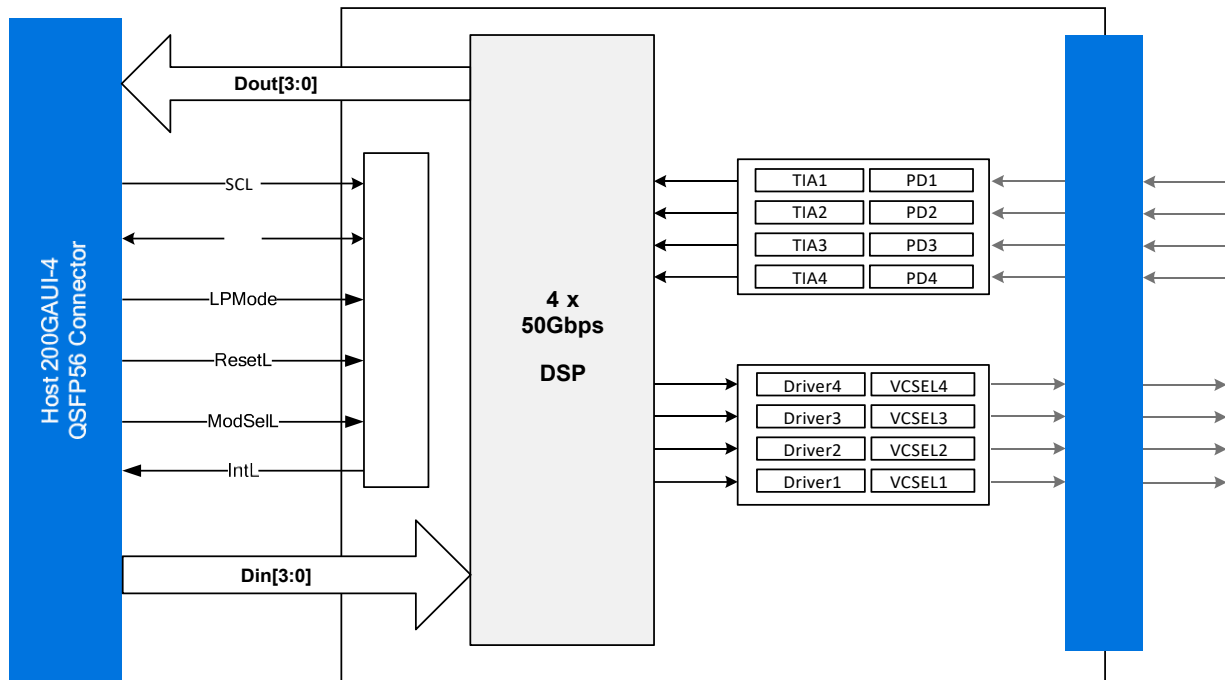


Figure 1: Transceiver Block Diagram

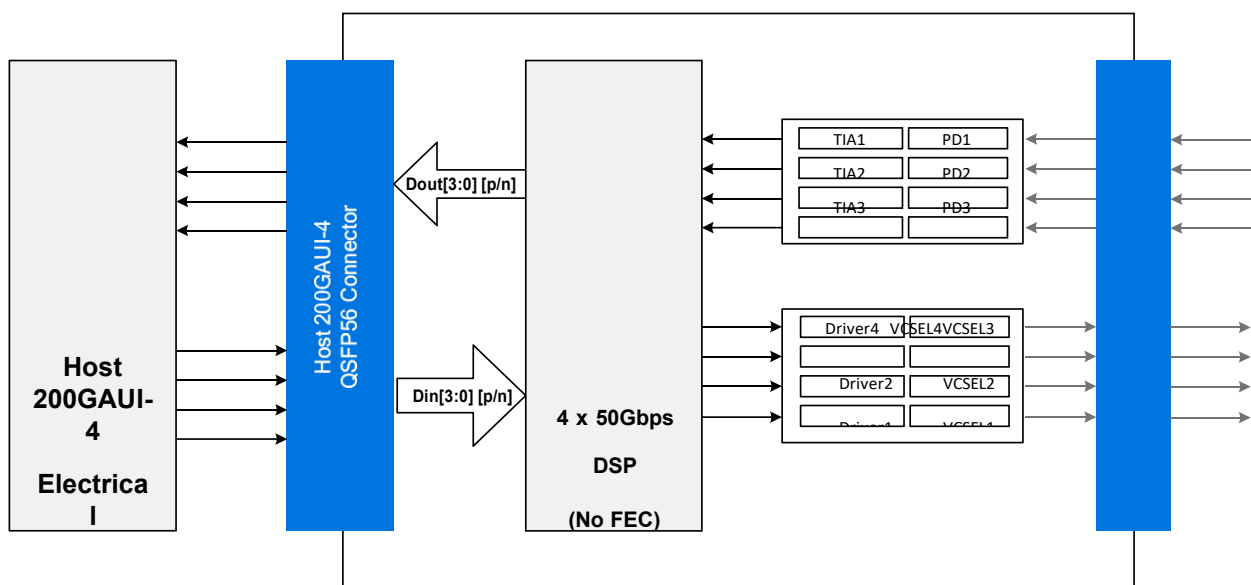


Figure 2: Application Reference Diagram

Transmitter

As shown in Figure 1, the transmitter path of the transceiver contains an 4x50Gbps 200GAUI-4 electrical input with equalization (EQ) block, integrated electrical multiplexer, VCSEL laser driver, diagnostic monitors, control and bias for the four modulator and multi-mode laser source. For module control and interrogation, the control interface (LVTTTL compatible) incorporates a Two Wire Serial (TWS) interface of clock and data signals.

Receiver

As shown in Figure 1, the receiver path of the transceiver contains four PIN photodiodes, trans-impedance amplifiers (TIA), integrated de-multiplexer and 4x50G 200GAUI-4 compliant electrical output blocks.

High Speed Electrical Signal Interface

The interface between QSFP-DD module and ASIC/SerDes is shown in Figure 2. The high speed signal lines are internally AC-coupled and the electrical inputs are internally terminated to 100 Ohms differential. All transmitter and receiver electrical channels are compliant to module 400GAUI-8 specifications per IEEE 802.3bs.

Control Signal Interface

The following pin is provided to control module or display the module status: ModSelL, ResetL, ModPrsL, IntL and LPMode. In addition, there is an industry standard two wire serial interface scaled for 3.3V LVTTTL. The definition of control signal interface and the registers of the serial interface memory are defined in the Control Interface & Memory Map section.

Handling and Cleaning

Exposure to current surges and overvoltage events can cause immediate damage to the transceiver module. Observe the precautions for normal operation of electrostatic discharge sensitive equipment; Attention shall also be paid to limiting transceiver module exposure to conditions beyond those specified in the absolute maximum ratings.

Optical connectors include female connectors. These elements will be exposed as long as the cable or port plug is not inserted. At this time, always pay attention to protection.

Each module is equipped with a port guard plug to protect the optical port. The protective plug shall always be in place whenever the optical fiber is not inserted. Before inserting the optical fiber, it is recommended to clean the end of the optical fiber connector to avoid contamination of the module optical port due to dirty connector. If contamination occurs, use standard MPO port cleaning methods.

Absolute Maximum Ratings

Exceeding the absolute maximum ratings table may cause permanent damage to the device. This is just an emphasized rating, and does not involve the functional operation of the device that exceeds the specifications of this technical specification under these or other conditions. Long-term operation under absolute maximum ratings will affect the reliability of the device.

Parameter	Symbol	Min.	Typical	Max.	Unit
Storage Temperature	Ts	-40		+85	°C
3.3 V Power Supply Voltage	Vcc	-0.5	3.3	3.6	V
Relative Humidity	RH	5		85	%

Recommended Operating Conditions^{*note3}

For operations beyond the recommended operating conditions, optical and electrical characteristics are not defined, reliability is not implied, and such operations for a long time may damage the module

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Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature*note4	Tc	0		70	°C
Power Supply Voltage	Vcc	3.135	3.3	3.465	V
Power Supply Noise*note5				25	mVpp
Receiver Differential Data Output Load			100		Ohm
Fiber Length (MMF)	OM3			70	m
	OM4			100	m

Note3: Power Supply specifications, Instantaneous, sustained and steady state current compliant with QSFP MSA Power Classification.

Note4: The position of case temperature measurement is shown in Figure 9.

Note5: Power Supply Noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels including peak-to-peak noise are limited to the recommended operating range of the associated power supply. See Figure 7 for recommended power supply filter.

General Electrical Characteristics*note6

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Parameter	Symbol	Min.	Typ.	Max	Unit
Transceiver Power Consumption				5	W
Transceiver Power Supply Total Current				1515	mA
AC Coupling Internal Capacitor			0.1		μF

Note6: For control signal timing including ModSelL, ResetL, IntL, LPMode, SCL and SDA see Control Interface Section.

Reference Points

Test Point	Description
TP1 and TP4	TP1 and TP4 are informative reference points that may be useful to implementers for testing components.
TP2	Unless specified otherwise, all transmitter measurements and tests defined in 802.3cd 138
TP3	Unless specified otherwise, all receiver measurements and tests defined in 802.3cd 138.

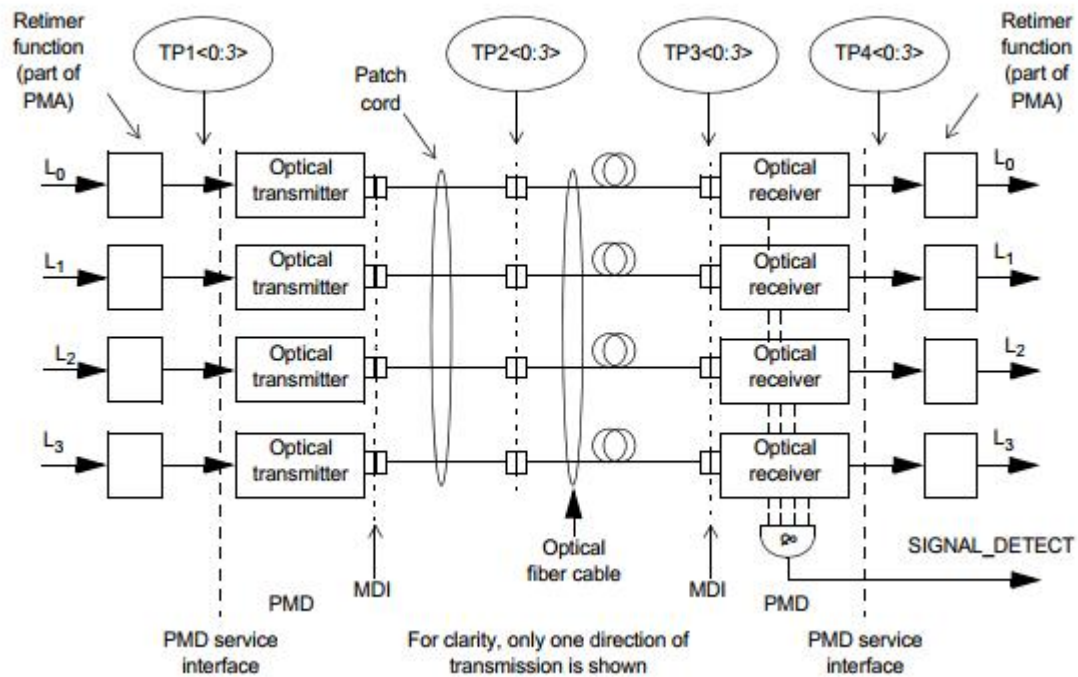


Figure 3: IEEE 802.3cd block diagram for 200GBASE-SR4 transmit/Receive paths

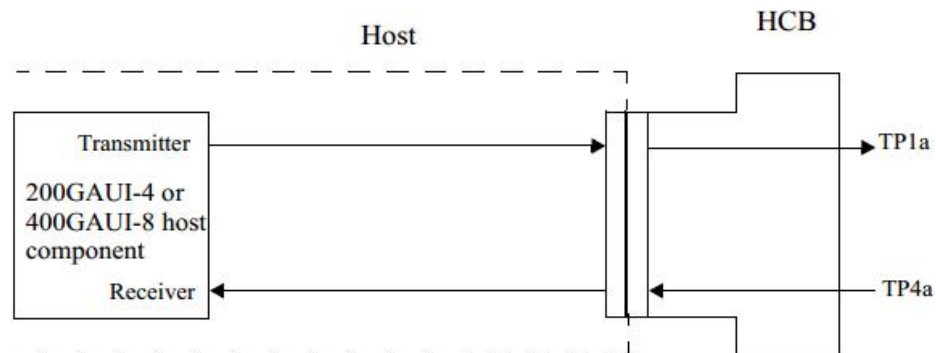


Figure 4: IEEE 802.3bs 400GAUI-8 compliance points TP1a, TP4a

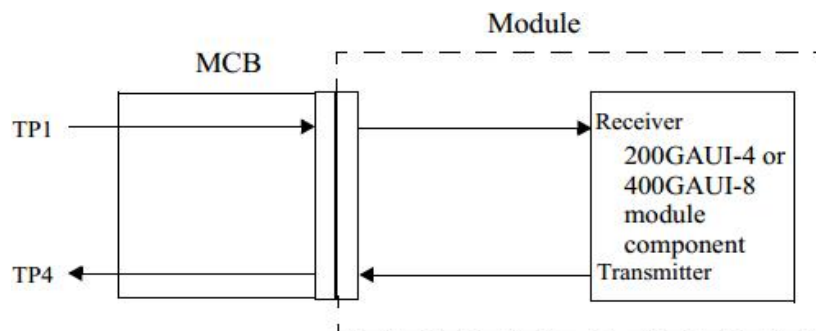


Figure 5: IEEE 802.3bs 400GAUI-8 compliance points TP1, TP4

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High Speed Electrical Input Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Parameter	Symbol	Min.	Typical	Max.	Unit
Signaling Rate, Per Lane (PAM4 encoded)	TP1		26.5625± 100ppm		GBd
Differential peak-peak Input Voltage Tolerance	TP1a	900			mV
Differential Input Return Loss (min)	TP1	Equation (83E-5) *9			dB
Common mode to differential return loss (min)	TP1	Equation (83E-6) *9			dB
Differential Termination Mismatch	TP1			10	%
Module stressed input test	TP1a				
Single-ended voltage tolerance range	TP1a	-0.4		3.3	V
DC common-mode output voltage*7	TP1	-350		2850	mV
Module stressed input test*8	TP1a				
Eye width			0.22		UI
Applied peak-peak sinusoidal jitter			Table 120E-6		
Eye height			32		mV

Note7: DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

Note8: Module stressed input tolerance is measured using the procedure defined in 120E-8 IEEE802.3-2018.

Note9: Equation (83E-5) and Equation (83E-6) refer to 802.3bs

High Speed Electrical Output Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Parameter	Symbol	Min.	Typical	Max.	Unit
Signaling Rate, Per Lane (range)	TP4		26.5625 ± 100 ppm		GBd
Differential peak-to-peak Output Voltage	TP4			900	mV
AC common-mode output voltage (RMS)	TP4			17.5	mV
Near-end ESMW	TP4	0.265			UI
Near-end Eye height, differential	TP4	70			mV
Differential Output Return Loss	TP4	Equation (83E-2) *10			dB
Common to differential mode conversion return loss (min)	TP4a	Equation (83E-3) *10			dB
Differential termination mismatch	TP4a			10	%

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Transition Time (20% to 80%)	TP4	9.5		ps
Common mode voltage	TP4a	-0.3	2.85	V

Note10: Equation (83E-2) and Equation (83E-3) refer to 802.3bs.

High Speed Optical Transmitter Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Optical Characteristics @TP2 Test Point

Parameter	Symbol	Min.	Typical	Max.	Unit
Signaling speed per lane			26.5625 ± 100ppm		GBd
Modulation format			PAM4		
Center wavelength	λ	840		860	nm
RMS spectral width	RMS			0.6	nm
Extinction ratio	ER	3.0			dB
Transmitter transition time, each lane				34	ps
Average launch power, each lane ^{*11}		-6.5		4	dBm
Outer optical modulation amplitude (OMA), each lane		-4.5		3	dBm
Launch Power in OMA-TDECQ		-5.9			dBm
TDECQ (PAM4), each lane				4.5	dB
TDECQ-10log ₁₀ (C _{eq}), each lane				4.5	dB
RIN _{12OMA}				-128	dB/Hz
Average launch power of OFF transmitter				-30	dBm
Optical return loss tolerance				12	dB
Encircled flux	19um	86%			
	4.5um			30%	

Note11: Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

High Speed Optical Receiver Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Optical Characteristics @TP3 Test Point

Parameter	Symbol	Min.	Typical	Max.	Unit
Signaling speed per lane			26.5625 ± 100ppm		GBd
Center wavelength	λ	840		860	nm
Damage threshold		5			dBm
Average receiver power per lane		-8.4		4	dBm
Receiver power, per lane (OMA _{outer})				3	

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Parameter	Symbol	Min.	Typical	Max.	Unit
Receive sensitivity (OMA _{outer}) per Lane (BER<2.4E-4)				*12	dBm
Stressed receiver sensitivity (OMA _{outer}) per Lane (BER<2.4E-4)				-3.4	dBm
LOS Assert (Avg.)	LOSA	-17			dBm
LOS De-Assert (Avg.)	LOSD			-10.5	dBm
Receiver reflectance				-12	dB

Note12: Receiver sensitivity (OMA_{outer})=max (-6.5, SECQ-7.9).

Regulatory Compliance Issues

Various standard and regulations apply to the SNR-QSFP56-SR4 modules. These include eye-safety, Component Recognition, RoHS, ESD, EMC and Immunity. Please note the transmitter module is a Class 1 laser product. See Regulatory Compliance Table for details.

Regulatory Compliance Table

Feature	Test Method	Performance
Laser Eye Safety and Equipment Type Testing 	(IEC) EN 62368- 1:2014+A11 (IEC) EN 60825-1:2014 (IEC) EN 60825-2:2004+A1+A2	CDRH Accession Number:2132182-000 TUV File: R 50457725 0001 CB File: JPTUV-100513
Component Recognition	Underwriters Laboratories (UL) and Canadian Standards Association (CSA) Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment	UL File: E317337
RoHS Compliance	RoHS Directive 2011/65/EU& (EU)2015/863	Less than 100 ppm of cadmium. Less than 1000 ppm lead, mercury, hexavalent chromium, poly brominated biphenyls (PPB), poly brominated biphenyl ethers (PBDE), dibutyl phthalate, butyl benzyl phthalate, bis (2-ethylhexyl) phthalate and disobutyl phthalates.
Electrostatic Discharge (ESD) to the Electrical Contacts	JEDEC Human Body Model (HBM)	High speed contacts shall withstand 1000V. All other contacts shall withstand 2000 V.
Electrostatic Discharge (ESD)		When installed in a properly grounded housing and chassis

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to the Optical Connector Receptacle	IEC 61000-4-2:2008	the units are subjected to 15kV air discharges during operation and 8kV direct discharges to the case.
Electromagnetic Interference (EMI)	FCC Part 15 Class B; CISPR 32 (EN55032) 2015;	System margins are dependent on customer board and chassis design.
Immunity	IEC 61000-4-3:2010; EN55035:2017	Typically shows no measurable effect from a 10V/m field swept from 80 MHz to 6 GHz applied to the module without a chassis enclosure.

Electrostatic Discharge (ESD)

The SNR-QSFP56-SR4 is complies with the ESD requirements described in the Regulatory Compliance Table. However, in the normal processing and operation of optical transceiver, the following two types of situations need special attention.

Case I: Before inserting the transceiver into the rack meeting the requirements of QSFP56 compliant, ESD preventive measures must be taken to protect the equipment. For example, the grounding wrist strap, workbench and floor should be used wherever the transceiver is handled.

Case II: After the transceiver is installed, the electrostatic discharge outside the chassis of the host equipment shall be within the scope of system level ESD requirements. If the optical interface of the transceiver is exposed outside the host equipment cabinet, the transceiver may be subject to equipment system level ESD requirements.

Electromagnetic Interference (EMI)

Communication equipment with optical transceivers is usually regulated by FCC in the United States and CENELEC EN55032 (CISPR 32) in Europe. The compliance of SNR-QSFP56-SR4 with these standards is detailed in the regulatory compliance table. The metal shell and shielding design of SNR-QSFP56-SR4 will help equipment designers minimize the equipment level EMI challenges they face.

Flammability

SNR-QSFP56-SR4 optical transceiver meets UL certification requirements, its constituent materials have heat and corrosion resistance, and the plastic parts meet UL94V-0 requirements.

QSFP-DD Transceiver Electrical Pad Layout

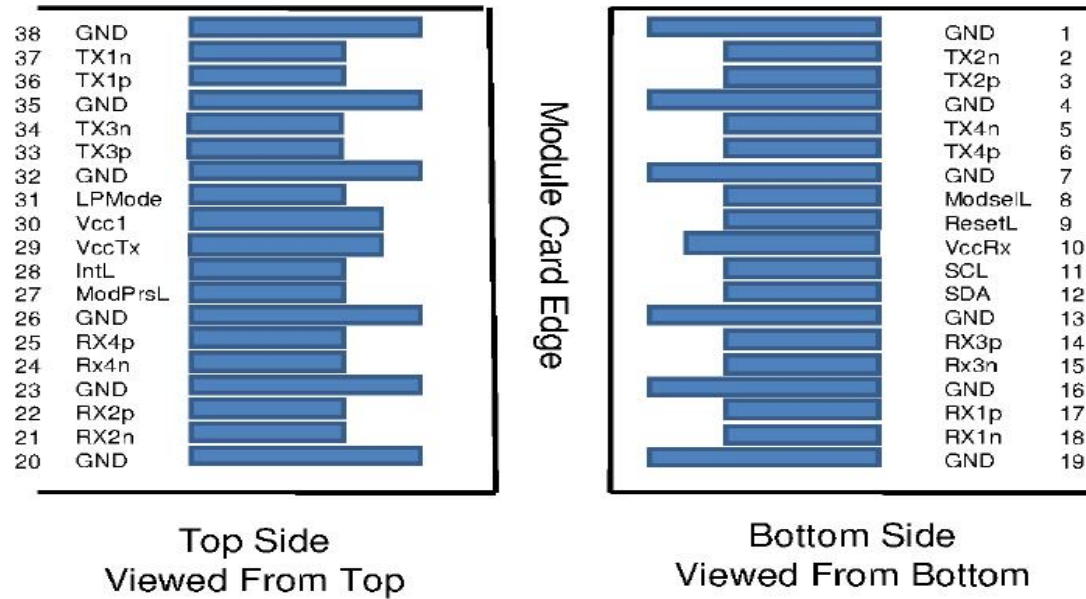


Figure 6: QSFP56 Module Pinout

Pin Arrangement and Definition

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		VccRx	+3.3V Power Supply Receiver	2	2
11	LVC MOS-I/O	SCL	2-wire serial interface clock	3	
12	LVC MOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	

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Pin	Logic	Symbol	Description	Plug Sequence	Notes
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		VccTx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMODE	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

1: GND is the symbol for signal and supply (power) common for the QSFP56 module. All are common within the QSFP56 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in SFF-8679 Table 6. Recommended host board power supply filtering is shown in Figures 7. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP56 Module in any combination.

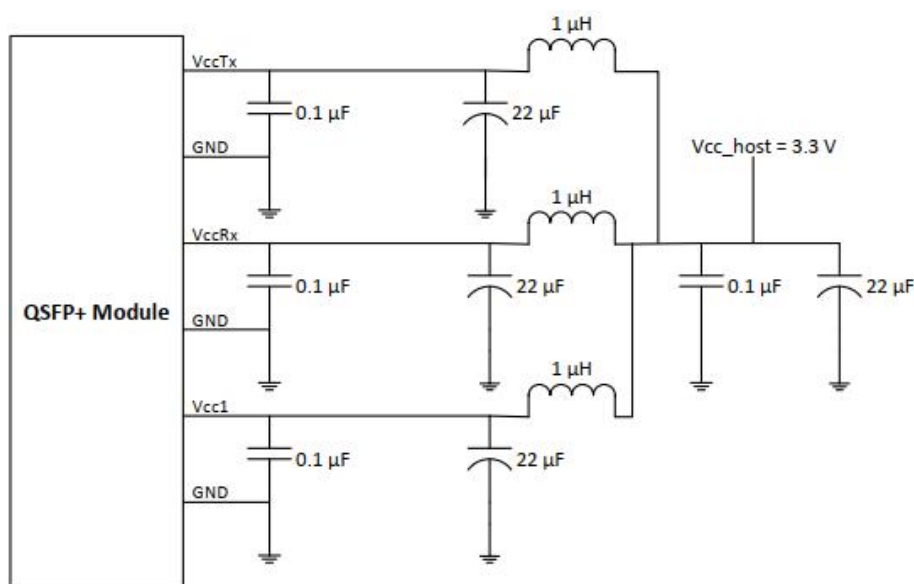


Figure 7: Host Board Power Supply Filter

During power transient events, the host should ensure that any neighboring modules sharing the same supply stay within their specified supply voltage limits. The host should also ensure that the

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intrinsic noise of the power rail is filtered in order to guarantee the correct operation of the optical modules. The reference power supply filter is shown in Figure 7.

Package Outline

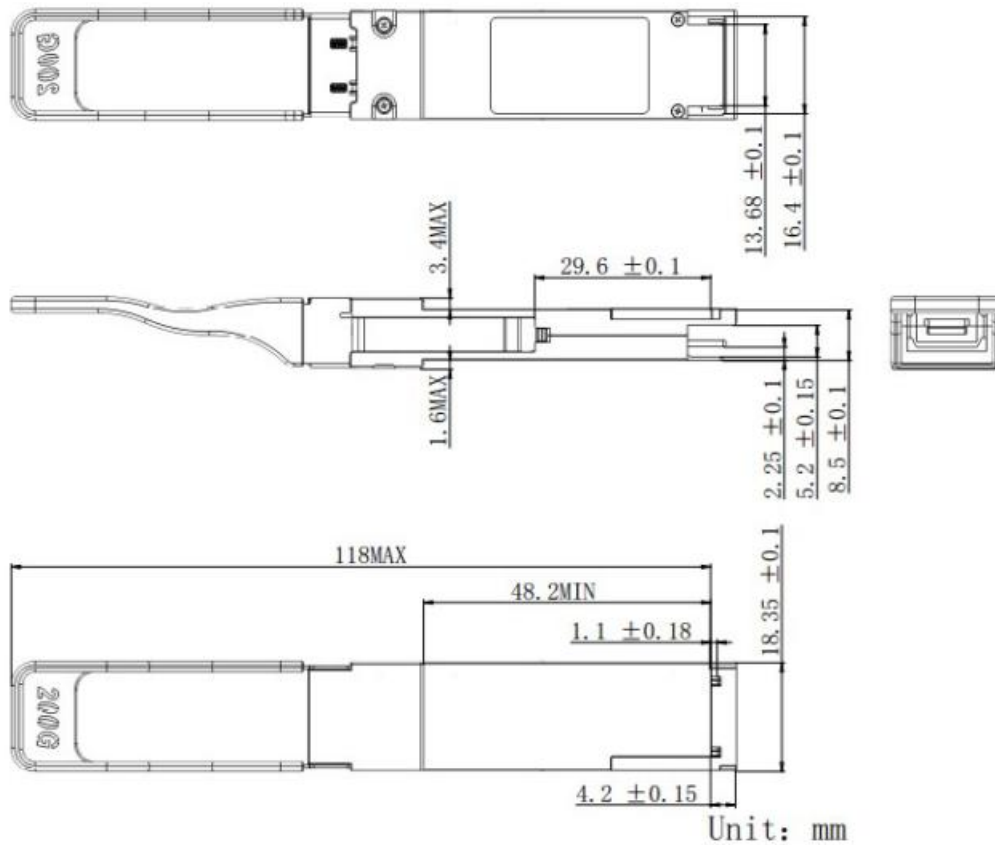


Figure 8: Mechanical Package Outline (All dimensions in mm)

*This 2D drawing is only for reference, please check with SNR before ordering.

The bellow picture shows the location of the hottest spot for measuring module case temperature. In addition, the digital diagnostic monitors (DDM) temperature is also calibrated to this spot.

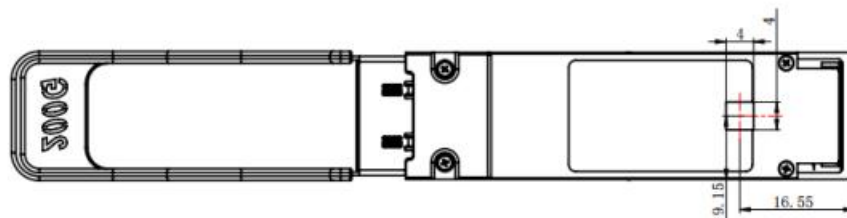


Figure 9: Case Temperature Measurement Point (All dimensions in mm)

The optical interface port is a male MPO-12 connector as specified in SFF-8436.

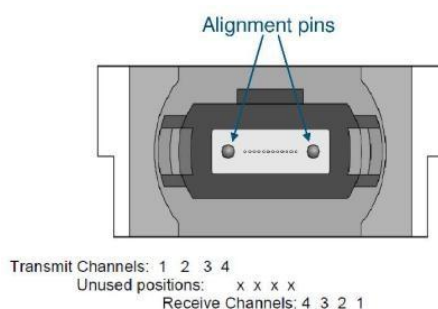


Figure 10: Module Optical Interface (looking into the optical port)

Control Interface & Memory Map

The control interface combines dedicated signal lines for ModSelL, ResetL, LPMode, ModPrsL, IntL with two-wire serial (TWS), interface clock (SCL) and data (SDA), signals to provide users rich functionality over an efficient and easily used interface.

SCL and SDA

SCL and SDA are a 2-wire serial interface between the host and module using the I2C protocols. SCL is defined as the serial interface clock signal and SDA as the serial interface data signal. Both signals are open-drain and require pull-up resistors to +3.3V on the host. The pull-up resistor value shall be 1.6k ohms for bus capacitive load 100pF, and 3k ohms for bus capacitive load 200pF.

This 2-wire interface supports bus speeds:

- Required - I2C SCL rates $\leq$ 400 kHz

SCL and SDA Pin Electrical Specifications

Parameter	Symbol	Min.	Typical	Max.	Unit
SCL and SDA	VOL	0		0.4	V
	VOH	VCC-0.5		VCC+0.3	V
SCL and SDA	VIL	-0.3		VCC*0.3	V
	VIH	VCC*0.7		VCC+0.5	V

ModSelL

ModSelL is an input signal. When held low by the host, the module responds to two wire serial communication commands. The ModSelL signal allows the use of multiple modules on a single two-wire interface. When ModSelL is high, the module shall not respond to or acknowledge any two-wire interface communication from the host. The ModSelL signal input node shall be pulled towards Vcc in the module. In order to avoid conflicts, the host system shall not attempt two-wire interface communications within the ModSelL de-assert time after any modules are deselected. Similarly, the host shall wait at least for the

period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-assertion periods of different modules may overlap as long as the above timing requirements are met.

ResetL

The ResetL signal shall be pulled towards Vcc in the module. A low level on ResetL initiates a complete module reset, returning all user module settings to their default state. During the execution of a reset (t_{init}) the host shall disregard all status bits until the module indicates a completion of reset interrupt by asserting "low" on the IntL signal. However, on power up (including hot insertion) the module should post this completion of reset interrupt without the host pulling ResetL low.

LPMode/TxDis

The LPMode pin is pulled up to Vcc in the QSFP56 module. This function is affected by the LPMode pin and the combination of the Power_override and Power_set software control bits (Address A0h, byte 93 bits 0,1). The module has two modes a low power mode and a high power mode. The high power mode operates in one of the four power classes.

When the module is in a low power mode it has a maximum power consumption of 1.5W. This protects hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.

The modules 2-wire serial interface and all laser safety functions must be fully operational in this low power mode. The module shall still support the completion of reset interrupt in this low power mode.

If the Extended Identifier bits (Page 00h, byte 129 bits 6-7) indicate a power consumption greater than 1.5W and the module is in low power mode it must reduce its power consumption to less than 1.5W while still maintaining the functionality above. The exact method of accomplishing low power is not specified; however, it is likely that either the Tx or Rx or both will not be operational in this state.

If the Extended Identifier bits (Page 00h, byte 129 bits 6-7) indicate that its power consumption is less than 1.5W then the module shall be fully functional independent of whether it is in low power or high power mode. The Module should be in low power mode if the LPMode pin is in the high state, or if the Power_override bit is in the high state and the Power_set bit is also high. The module should be in high power mode if the LPMode pin is in the low state, or the Power_override bit is high and the Power_set bit is low. Note that the default state for the Power_override bit is low.

IntL

IntL is an open-collector output signal from the module. It shall be pulled up towards Vcc on the host board.

Memory Map

The control interface and memory map of the QSFP56 module is compliant with the QSFP MSA.

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The QSFP56 module support I2C interface protocol defined by the SFF-8679. Access clock frequency support a minimum of 100 kHz with no clock stretching and burst read/write of at least 32 bytes.

The module meets the following requirements:

The module initialize in hardware mode when LPMode is de-asserted.

The transmitter is disabled when the module is held in reset.

Tx Squelch function is implemented as defined by the QSFP56 MSA. When squelched, the transmitter is disabled.

Rx Squelch function is implemented as defined by the QSFP56 MSA. When Rx CDR LOS is asserted, CDR output is squelched.

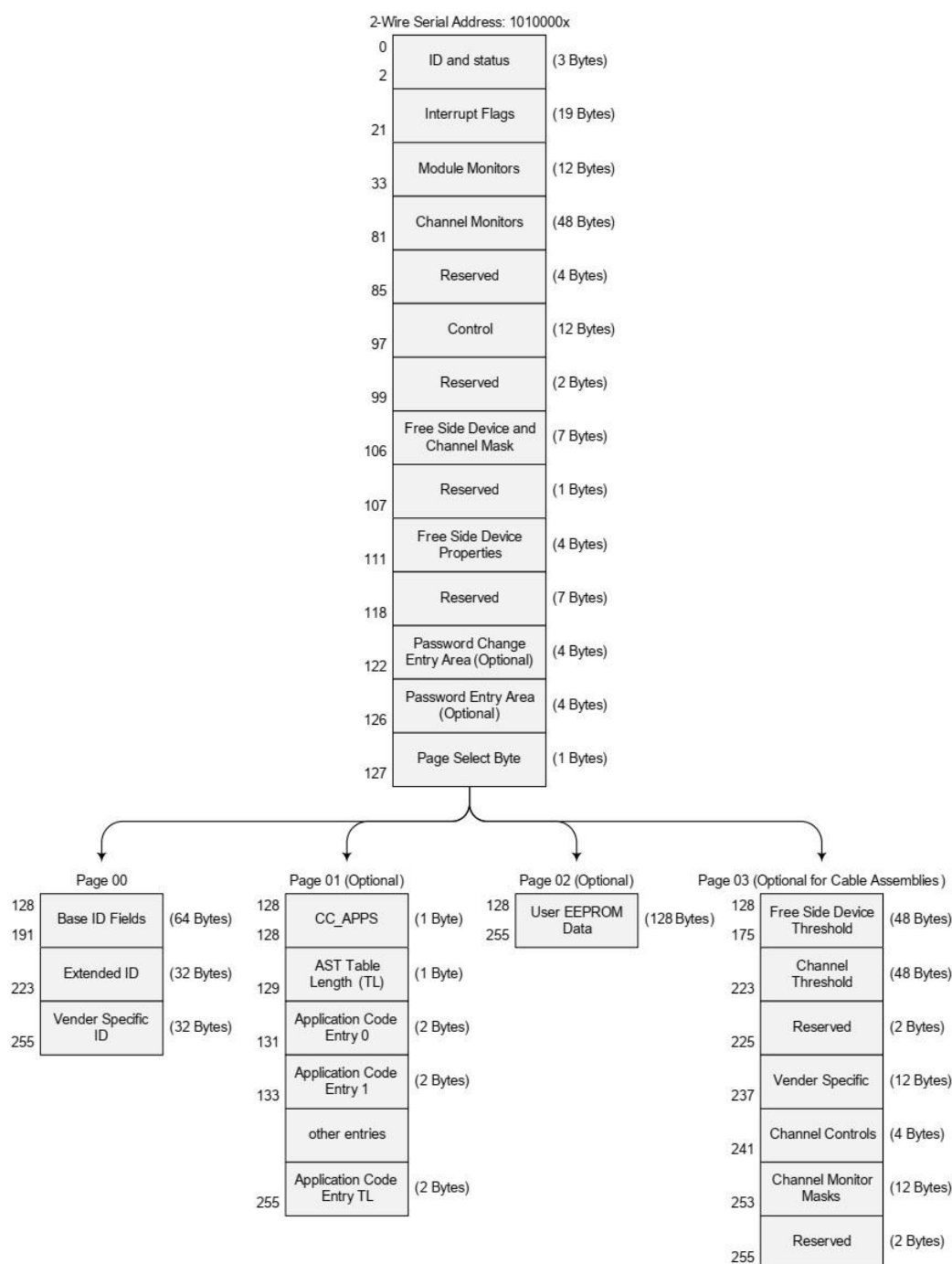


Figure 11: Simplified QSFP56 SFF-8636 Module Memory Map Architecture

GUARANTEE:



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